

Reducing Time to Volume and Time to Market: Is Silicon Debug and Diagnosis the Answer ?

Organizer: Mike Ricchetti, Intellitech

Moderator: Fidel Muradali, Agilent

Panelists: Bart Vermeulen, Philips
Bulent Dervisoglu, Cadence
Bob Gottlieb, Intel
Bernd Koenemann, IBM
CJ Clark, Intellitech

Abstract

Advances in semiconductor technology and design automation, together with increased market competition, have driven engineers to achieve higher levels of integration, with shortened development cycles. Consequently, verification and analysis are becoming a major bottleneck for timely design of complex systems. The panelists and the audience will explore silicon debug and its impact on the design cycle.

Some the questions to be addressed during this panel session are as follows:

- What is silicon debug ? What does it involve ?
- Why do we care about silicon debug ? Why do it, what does it cost/save in terms of dollars, time to market etc. ?
- How big of a problems is it ? How important is it (value proposition) ?
- What is being debugged ? Functional escapes from pre-silicon verification, electrical problems, process problems, etc. ?
- What sort of hardware hooks (design for debug/test) and tools are needed ?