

Special session (Innovative Practices Track)

Validation & Test of Network Processors and ASICs

Presenters: Faraydon Karim, ST Microelectronics
Haluk Konuk, Broadcom
Keesup Kim, Intel

Organizer: Sujit Dey, UC San Diego
(dey@ece.ucsd.edu)

Abstract

Rapid growth in the internet and enterprise network traffic, need by both subscribers and operators to provide for differentiated services, and the constant evolution of wireline and wireless networking functions, algorithms and standards, is leading to a high demand for ultra high speed, yet programmable, network processors and ASICs. This session will introduce the design of network processors, and highlight important validation and test challenges associated with network processors and ASICs.

The first speaker in this session will review the architecture of a typical OC-192 network processor – a highly complex system-on-chip, consisting of multiple processors, specialized hardware blocks, multiple high-speed embedded memory units, and a highly concurrent and complex on-chip interconnect structure. The talk will analyze the validation and manufacturing test problems of hardware-software GHz network processor chips, which have to use aggressive architecture designs and nano-meter technologies to obtain the required multi-GHz speed, while relying on the presence of multiple processors to provide the necessary flexibility.

The second talk will address testing of embedded GHz network processors. In particular, it will describe the challenges faced in testing a specific high-speed low-power network processor chip, which includes two custom-design 64-bit MIPS processors, 0.5MB of L2 cache, and multiple high speed communication blocks, such as gigabit-ethernet, hyper-transport, and double-data-rate memory controllers. Some test solutions will be presented, and major test challenges that need to be addressed will be listed.

The third talk in this session will address the problem of delay testing in communications chips. In communication devices such as network switches and routers, there usually are multiple unrelated clocks controlling various interfaces and logic. These multiple clock domains presents unique challenges in production testing since it becomes very difficult to predict when the expected output will show up at the pin boundary. The talk will show why delay defects need to be addressed, and how to deal with cycle uncertainty problem during production testing. It will present a novel compaction technique used to deal with the test data volume explosion resulting from including of delay defect screening tests.