

# Multi-GigaHertz Testing Challenges and Solutions

Karim Arabi<sup>1</sup>, Klaus-Dieter Hilliges<sup>2</sup>, David Keezer<sup>3</sup> and Sassan Tabatabaei<sup>4</sup>

<sup>1</sup> PMC Sierra, Inc., 8555 Baxter Place, Burnaby, British Columbia, Canada V5A 4V7

<sup>2</sup> Agilent Laboratories, 3500 Deer Creek Road, Mailstop 24M-A, Palo Alto, CA 94304-1392

<sup>3</sup> The School of Elec. & Comp. Eng., Georgia Institute of Technology, Atlanta, GA 30332-0250

<sup>4</sup> Vector 12, Inc., 13353 Commerce Parkway - Suite 2143, Richmond, BC, Canada V6V 3A1

**Abstract:** *The advent of terabit aggregate rate telecommunication devices and multi-gigahertz I/O interfaces is posing new challenges on the semiconductor and ATE industries. Telecom chipmakers are currently using ad hoc techniques to test these kinds of devices due to the lack of a credible commercial solution. This session highlights the challenges of testing multi-gigahertz interfaces and presents promising early solutions.*

## Introduction

With the broad deployment of advanced interface definitions of 3GIO, Infiniband, Rapid-IO, HyperTransport and others we are facing a profound technology and architectural change in the segment of computation ICs: synchronous or source-synchronous buses are going to be replaced by high-speed serial interfaces. These embedded clock interfaces that are well known for communication devices have advanced not only in terms of performance, but also more importantly in density, power consumption and in the ability to be implemented in mainstream CMOS processes. As a result highly integrated SOCs will be equipped with large numbers of these serial links enabling processing of high-bandwidth data-streams in communication and computation systems. One can envision highly complex network processors that primarily interface through 2.5Gbps up to 10Gbps signal pins. Embedded clock interfaces challenge traditional test approaches in various ways: High-speed test data sequencing, high timing accuracy of the ATE and sufficient signal integrity of the DUT-interface would be prerequisites for functional and timing testing. However, on top of these stringent requirements, generally these embedded clock interfaces demand the ATE receiver to track the signal's phase as well as to handle non-determinism in the bit-stream. For today's 2.5Gbps standalone SerDes these effects can be overcome by traditional searching of the eye sampling point or by matching to bits. ATE equipment initially developed to test advanced source-synchronous buses can be deployed to test these interfaces. Nevertheless, the future of integrated 10Gbps CMOS implementations may make these traditional approaches unfeasible.

## Potential Solutions

One possible solution is to combine multiple ATE channels to provide effectively high rate test data patterns by careful edge placement and using under sampling and time interleaving techniques to increase the effective test data sampling rate. Major limiting factor is the timing skew between adjacent ATE channels and the bandwidth of each channel.

Today, design and test engineers often resolve to non-ATE based test solutions to avoid these difficulties such as using a BIST technique comprising internal or external loopback of on-chip generated test data. However, these methods do not allow measuring ever tighter timing specs (e.g. jitter generation and jitter transfer) that eventually can not be guaranteed by design any longer. To address these drawbacks, high accuracy timing measurement circuitry can be implemented on-chip to provide the capability of measuring timing specifications at multi-gigahertz frequencies. A practical solution needs to address issues such as on-chip noise, off-chip control access, low area overhead, high-speed signal routing, traceability, and support for multiple channels.

Another possible strategy is to divide the test challenge into bit-stream testing and timing parametric tests and addresses them independently. ATE can be required to enable random data I/O (bit-stream test) through the high-speed serial interfaces to enable high throughput functional or structural testing of the SoC. This may demand clock and data recovery circuitry for each ATE receiver and other innovative schemes to track the DUT's bit-stream. Certainly, DFT and specific test approaches will be required to make the bit-stream sufficiently deterministic to enable single shot pass/fail testing.

## Conclusion

No single solution is currently addressing all challenges of testing multi-gigahertz interfaces. A paradigm shift in the way ATEs communicate with chips is a must. The ultimate solution will be the result of innovations in ATE design and on-chip DFT techniques.