

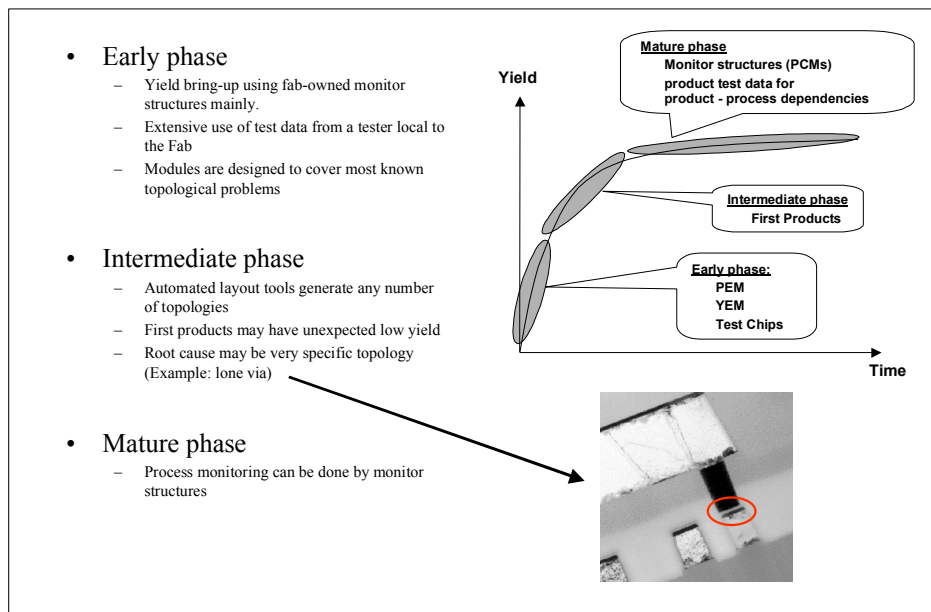
Special Panel Session

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Test as a key enabler for faster yield ramp-up

The successful introduction of a new IC manufacturing process requires a rapid yield ramp. In-line inspection, parameter evaluation using special tests structures and memory arrays are typically used to debug and diagnose a new process or product.

However, not all the failure mechanisms can be anticipated and detected using such test structures and memory blocks. Logic structures have a different and irregular topology, which may lead to different defect sensitivities. Indeed, some of the (spot) defects may not occur in the test structures or memories and may then only be detected at the product's final wafer test. Retest, precise electrical fault diagnosis methods and advanced (physical) failure analysis procedures are then needed to localize and characterize these types of failures.



The discussions in the panel session will focus on how test techniques can help to ramp-up the yield during early fabrication phases and how test can continue improving the yield throughout the product life cycle.

A specific focus will be given to diagnosis techniques, and to the question what needs to happen for the industry to get the point where fast, on-line diagnosis can be used to obtain and accurate results.