

## **Panel Session 8:**

### **Microprocessor Test and Validation, Any New Avenues?**

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**Abstract:**

The annual rate of increase in microprocessor performance in the last dozen years surpasses technology-driven performance improvements. Such excess performance improvements have been achieved through highly complex control of redundant information and units. While the complex control has provided performance improvements, it has resulted in challenging test and validation issues.

As novel validation techniques attempt to exploit behavioral information and representation, it is becoming evident that traditional test approaches are limited in the microprocessor domain by exacting area, performance, test application and generation time constraints. High volume manufacturers face tight area constraints, while critical control paths frequently leave no room for incorporation of traditional design-for-test techniques. New alias modes result when redundant information and units enable, in the face of fault manifestation, limited self-healing, albeit at reduced performance.

Are we reaching an era in the microprocessor domain, wherein quantitative changes are heralding fundamental test approach realignments? Our panelists will provide answers to this question in the domain of microprocessor test by discussing:

- a) Test and validation challenges facing the microprocessor industry today
- b) Current test and validation techniques used in industry
- c) New research in industry and academia
- d) Test impact of functional and behavioral information and representation
- e) Possible cross-pollination between test and verification techniques
- f) Future directions in microprocessor test

The panel will be composed of four to five members from leading microprocessor companies and one participant from academia, all active in state-of-the-art microprocessor test research and development.