

Panel Session 4:

ATE for VLSI: What Challenges Lie Ahead?

Coordinator:

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Moderator:

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Panelists:

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Abstract:

Recently observers have noted that the SEMI roadmap for ATE presents some disquieting demands — even that ATE may be “the show-stopper.” Escalating pincount, electrifying speeds, excruciating accuracy and megagate complexity make traditional VLSI ATE unbearably expensive. The question put to these panelists is, quite simply: “Is there a way out?”