Panel Session 2:

Will 0.1 um CMOS Digital Circuits Require Mixed-Signal Testers?

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Abstract:

Digital CMOS technology is rapidly evolving to deep sub-micron. Interconnect wires are treated as resistors, and edge capacitance is greater than area capacitance. On a per gate basis, Iddq is increasing 10X every three years and operating current is decreasing. Clock frequencies are approaching the 'black art' region of 1 GHz, and the signals look like sine waves.

Will digital testing become mixed-signal testing when we reach 0.1 um gate lengths in five years? For digital circuits, what analog (non-deterministic) tests will be needed: frequency response, time domain reflectometry, signal to noise ratio, bit error rate, power supply rejection ratio, distortion, offset, etc.?

Will digital testers simply become obsolete, even if they can deliver bits fast enough? Will non-digital IC test data be converted on-chip to allow use of digital testers? Hold onto your spectrum analyzers!

A new format will be introduced: after each person gives a 5 minute position statement, the two teams will debate the topic, spurred on by questions (and answers) posed by the audience. To conclude, the audience will vote for the answer (yes/no), and the winning team will receive prizes.