

Panel Session 1:

Systems On Silicon Design And Test Challenges

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Abstract:

Since the early 70's, chip complexity has been continuously growing at a rate that has never slowed down, targeting the gigabit complexities for DRAM around the year 2000. The consequence of such an evolution is the capability to put tenths of millions of transistors today and hundreds of millions of transistors tomorrow in a single chip.

In this context the design and test challenges are various:

- Designing for such complexities, using system level design methodologies going from the behavioral level down to silicon (that means, software-hardware co-design, advanced floor planning and complex validation approaches).
- Power conscious design (that means designing with data throughput constraints within the chip and minimizing power consumption with low-voltage, high-speed optimization of the device behavior).
- On these levels of complexity reusability of functions coming from multiple sources is imposed by the design economics, with the WIN vision as the long term perspective. Capitalizing on intellectual property is becoming of major importance to address the new, emerging markets like multimedia, where experiences from various market segments should be reused in a single system on a chip. IP standardization is then another critical requirement to solve the huge list of challenges created by the system on chip perspectives.
- In recent IC examples large memory arrays occupy more than 50% of the IC area and include more than 80% of the transistors. Since large memories are very tight on the process limits they will include the large majority of defects.

What test and repair techniques should be used to avoid high defect levels and low yield ?

Available test sets for cores have to be applied to the I/Os of the embedded core. But the complexity of the test sequences and the length of the scan chains is a serious limitation for scan-path approaches.

- What are the best DFT/BIST solutions for embedded cores ?
- Use of cores from external sources raises some other questions. Who is responsible for the core testability ? What are the implications of IP protection issues on core testability ?

These and other design and test challenges including IP issues and standardization, standardization issues for core testing, DFT for high speed parts, and testability of analog parts, will be debated by specialists coming from the design and test community.