

Panel Session 8

Hardware-Software Co-Design for Test: It's the Last Straw!

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Panelists:

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Abstract:

High-level synthesis, the process of automatically generating a logic description of a design from its behavioral description, has seen a lot of developments in the past few years, and some new commercial tools have appeared on the CAD market. In the computer-aided testing (CAT) area, high-level synthesis for testability, which aims to automatically produce testable designs from their high-level description while still being a research domain, has produced some interesting results in recent years.

When addressing the system level, specially embedded systems — the system specification is generally provided at a higher level of abstraction and the system implementation has to be split according to a set of constraints into pieces of software running on standard processors on the one hand and specialized, application-specific hardware on the other hand — both parts exchanging data use communication interfaces.

To automate the design of such systems, hardware/software co-design methods are used, which main tasks are the partitioning process of the system specification into parts to be implemented in software and parts to be synthesized into hardware, and the synthesis of the communication process between the system modules. The development of hardware/software co-design platforms is still a research task, even though some prototypes are currently under commercialization.

In the CAT area, the design of testable and reliable embedded systems is only a starting research topic. Hardware/software co-design for testability and reliability is therefore a very young field, but one that is driven by current industrial needs. On the other hand, embedded system design poses new challenges that are not yet currently being met by any set of tools known to existing commercial vendors. Even worse, embedded systems will often be used in safety-critical applications, such as automotive, avionics, industrial control, or telecommunications. This has an enormous effect on system design requirements for testability and reliability.

The objective of this panel session is to analyze the problem of hardware/software co-design for testability and reliability from different points of view, among them being the relationship of this process with other issues or topics. The main points to be discussed during this panel session will be the relationship between test standards and system tests. The concept of

partitioning for testability and reliability will also be discussed. In addition, the panelists will examine exactly what concepts like BIST and fault tolerance mean at the hardware/software system level, and how this can interact with high-level synthesis for testability. Finally, there will be a discussion regarding whether or not there is a need to mix software testing techniques and hardware testing techniques.

This panel session brings together specialists who can address these questions, give their own views, and provide valuable information based on their own experiences. The participation of CAD and CAT vendors, as well as professional users from the telecommunications and avionics fields, will bring the added value of examining the industrial needs and viewpoints.