

Panel Session 6

Delay Fault Testing: How Robust are Our Models

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Abstract:

This panel will debate fundamental concepts in delay fault testing. A basic assumption in delay fault testing is that for a given transition propagated along a path, the path delay does not depend on values and transitions at circuit nodes that do not belong to the path. Is this assumption justified? If not, as some panelists will argue, then our current test procedures may miss some of the faults they target, and a lot of the current work in robust delay fault testing and in the synthesis of robust-testable circuits may be unreliable.

A related question to be debated by the panel is whether a circuit passing a complete set of robust path delay tests at clock period T is guaranteed to perform its intended function at any clock period $\geq T$. What are the delay models for which the answer is always true? What are the limitations of these models? Do we need to change the way we test circuits for delay faults?

Other important questions deal with the hardware generating the tests: Can the response to the test be measured in a meaningful way (from a timing point of view)? Is the generating hardware capable of applying all two-pattern tests? What delay model should be used to have a reasonable trade-off between accuracy and practicality?