

## Panel Session 5

### BIST: Advantages or Limitations?

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#### Abstract:

BIST has claimed many advantages in reducing IC test costs. For example, implementing BIST hardware on-chip is reported to reduce ATE costs. However, if one is still going to perform IC parametric tests — including extended Iddq tests and possibly functional tests — does it really result in significantly reduced testing costs? It has been claimed that the use of pseudo-random pattern-based BIST can reduce test generation effort and so reduce not only test generation costs, but also time to market. However, given the reality of pseudo-random pattern resistance in practical circuits, is the fault coverage achieved really adequate? Or, is the time saved in test generation reduced considerably by the effort required to design for pseudo-random pattern testability and/or by the time required to perform signature simulation and fault simulation?

This panel will look at BIST's claimed advantages and examine whether or not, or how often, these advantages are achieved in practice. It will also attempt to address the question: Are some of BIST's claimed advantages really limitations? For example, the application of random-pattern tests at speed may cause a lot of activity in the circuit (and therefore may be effective at detecting non-classical faults), but what effect does this have on power dissipation and power management design considerations?