

Panel Session 4

Design Validation: Formal Verification vs. Simulation vs. Functional Testing

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Abstract:

For today's complex designs with heterogeneous implementation platforms, design validation becomes more critical and more difficult than ever, consuming a significant portion of the design cycle. Validation needs to be done, not only for the behavioral/RT-level specification that has been written from very abstract specification of the design intent, but also through the various design steps from high-level to physical-level design.

The methodology used overwhelmingly today in the design houses to validate design intent and implementation is simulation, and in some cases, emulation. However, because of its inherent ad-hoc nature, simulation/emulation-based validation may require several iterations of error detection and design modification. Also, simulation/emulation suffers from an inherent lack of being inconclusive, apart from being unacceptably slow or prohibitively expensive.

A rising tide of formal verification techniques promises to solve the validation problem conclusively. However, even though formal verification techniques have been successfully applied to control parts of a design for which state transition graphs exist, it has yet to be applied to data-path parts. Some recent work on formal verification techniques for arithmetic circuits and processors raises the hope of formal verification being the solution, but it is still far from being applicable to entire systems.

More recently, it has been shown that test pattern generation techniques for manufacturing defects can be utilized to test for design errors also, thereby providing an alternative methodology for design validation. Automated generation of testbenches, combined with simulation and analysis, can make the process of design validation faster and more deterministic — while still being applicable to complex systems.

While classical functional methods such as OBDD-based techniques have not been effective for designs approaching multimillion transistors, new hybrid methods combining structural (ATPG-based) and functional methods, need to be examined.

This panel will discuss all of the techniques that are available and in use today to help in the complex design validation task. The panel will probe what the deficiencies are and what evolving methodologies look promising for tomorrow's challenging design validation tasks. The panelists will address whether any of the current methodologies is sufficient by itself, or if the future holds a need for hybrid methods.

The question is, can functional testing help solve the design validation problem, providing a middle-of-the-road solution between simulation/emulation and formal verification?