

## Panel Session 2

### Is High Frequency Analog DFT Possible?

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#### Abstract:

Design For Test (DFT) means altering a circuit design to make it more testable. DFT for high frequency (>100 MHz) analog integrated circuits seems destined to be limited to loop-around testing and other such end-to-end test methods. Any circuitry used to modify, monitor, or inject signals into the middle of such circuits inevitably impacts the function's performance greatly — much more than for low-frequency circuits. Most papers proposing general DFT methods do not discuss frequency limits to their approach.

A panel discussion at VTS '94 addressed RF test strategies, and it was apparent that RF testing is a complex field (no pun intended), which could benefit from more DFT.

Panelists from universities and industry will address their answers to the following questions:

- Will improving the testability of HF analog circuits be limited to selection of the best stimulus and output analysis, or is it practical to modify HF elements of an IC design to make it more testable?
- Does the small number of transistors in typical HF analog circuits justify adding any internal test circuitry at all?
- What are the frequency limits of existing analog DFT approaches (analog bus, re-configuration, loop-around, etc.)?