

Wednesday Afternoon Plenary Talk
Title: Optimizing SoC Manufacturability
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Abstract

Every new semiconductor technology node provides further miniaturization and higher performance, thus increasing the functions that electronic products could offer. Although adding such new functions do benefit the end-user, but they also necessitate finer and denser semiconductor fabrication processes, which make chips more susceptible to defects. Today's nanometer technologies are reaching defect susceptibility levels that result in lowering the manufacturing yield and reliability, and hence lengthening the production ramp-up period, and therefore the time to volume (TTV). The impact on manufacturability and TTV is very critical for the semiconductor industry. It puts the conventional IC realization flow at an impasse. In fact, every single phase in the IC realization flow has an impact yield and reliability, including the design phase, prototyping, volume fabrication, test, assembly, packaging, failure analysis and even the post-production life cycle of the chip. In order to optimize yield and reach acceptable TTV levels, the semiconductor industry needs to adopt advanced manufacturability optimization solutions. These solutions need to be implemented at different phases of the chip realization flow.

The conventional semiconductor manufacturing infrastructure, i.e. the external equipment and processes, alone are insufficient to handle such advanced solutions; supplemental on-chip infrastructure is needed. To optimize manufacturability, the industry has recently introduced a range of embedded intellectual-property (IP) blocks, called infrastructure IP. These are meant for inclusion into IC design and utilized during the different phases of product realization.

Semiconductor IP is well known for the last decade. Most of the known IP blocks, though, are functional ones, such as embedded processor, memory, analog, or FPGA cores. Whereas, Infrastructure IP (I-IP) is not functional, i.e. does not contribute to the normal functionality of a given IC. Rather, I-IP is embedded in an IC solely to ensure its manufacturability and lifetime reliability. This role is similar to the infrastructure elements of a building, such as wiring networks or plumbing, which are independent from the actual function of the building.

This keynote introduces the key trends and challenges resulting in manufacturing susceptibility and field reliability that necessitate the use of such Infrastructure IP. The keynote discusses the yield optimization loops. And then, it concentrates on several examples of Infrastructure IP for process monitoring, test & repair, debug & diagnosis, timing, and fault tolerance, while demonstrating their effectiveness in improving yield and reliability.

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Yervant Zorian is the Vice President and Chief Scientist of Virage Logic Corp. He serves on the Board of Directors of several public companies and private start ups. Previously, he was the Chief Technology Advisor of LogicVision Inc. and a Distinguished Member of Technical Staff at AT&T Bell Laboratories. He served on the Board of Directors of Virage Logic Corp from its initial development phases, through its successful initial public offering in 2000.

Dr. Zorian received the MSc degree in Computer Engineering from the University of Southern California and a PhD in electrical engineering from McGill University. He also holds an executive MBA from Warthon School of Business. He is the author of over 200 technical papers and three books, received

several best paper awards and holds over a dozen U.S. patents. Dr. Zorian serves as the Editor-in-Chief Emeritus of the IEEE Design & Test of Computers and participates in editorial advisory boards of IEEE Spectrum, and JETTA. He chaired the Test Technology Technical Council of IEEE Computer Society, and founded IEEE P1500 SECT Standard Working Group. He is a Golden Core Member of IEEE Computer Society, Honorary Doctor of National Academy of Sciences of Armenia and a Fellow of the IEEE. He was recently selected by EE Times among the top thirteen influencers on semiconductor technology.

Dr. Yervant Zorian joined the Virage Logic management team as Vice President and Chief Scientist in 2000. Since 1996, Dr. Zorian has served as Chief Technical Advisor of LogicVision. Prior to that, Dr. Zorian served as a Distinguished Member of the Technical Staff at Lucent Technologies, Bell Laboratories. Dr. Zorian is the Vice President of the IEEE Computer Society for Technical Activities and is the Editor-in-Chief Emeritus of IEEE Design & Test of Computers. He founded and presently chairs the IEEE P1500 standardization working group for embedded core test, and has authored over 200 papers and three books. Dr. Zorian has received a number of best paper awards, is an honorary doctor of the National Academy of Sciences of Armenia, and a Fellow of IEEE. Dr. Zorian received an MSc degree from the University of Southern California, and a PhD from McGill University.