

## VLSI Design: Tuesday Keynote Address



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### **65nm Omnibudsman**

#### *Abstract*

Just as the semiconductor industry has begun to ship production products at 90nm we find ourselves starting "Pipe Cleaner" designs at 65nm. Each process generation provides both opportunities and challenges to design teams and the 65nm node is no exception. This talk will provide a short overview of the challenges of designing at 65nm with special emphasis on the relationship of the design process to the manufacturing process and what is changing in the way that design tools keep complexity at bay in a world where power density and process variability threaten to drive us off of Moore's now famous law.

*Ted Vucurevich serves as a Cadence Chief Technology Officer, reporting to Michael J. Fister, President and CEO. He is responsible for driving advanced research and development and directing Cadence Laboratories. In addition, he serves as an executive fellow.*

*In his prior role as chief architect at Cadence, Vucurevich helped develop the strategies and technology initiatives in system-on-a-chip (SoC)-based design, DSM infrastructure, software interoperability, design methodology development, and Internet-based electronic system design.*

*Vucurevich joined Cadence in 1992 as director of the Analog Physical Design group. In 1994 he was promoted to work as an architect in the Viper Development group. He was later named chief architect and held that position for five years. Prior to Cadence, Vucurevich worked 14 years at Analog Devices where he held roles in product, design, and computer-aided design (CAD) engineering. He was a co-founder of the Linear Signal Processing Division, where he was responsible for the implementation of a complete mixed-signal ASIC CAD environment.*

*Vucurevich received his bachelor of science degree in electrical engineering from the University of Arizona.*

## Embedded Systems: Tuesday Keynote Address