

Tutorial: Architectural, System Level and Protocol Level Techniques for Power Optimization for Networked Embedded Systems

Speakers

Luca Benini, Universita, De Bologna, Italy

Sandeep K. Shukla, Virginia Tech, USA

Rajesh K. Gupta, University of California at San Diego, USA

Dynamic Power Management (DPM) entails employing strategies that yield acceptable trade-off between power/energy usage and their performance penalties. These include heuristic shutdown policies, prediction-based shutdown policies, multiple voltage scaling and stochastic modeling based policy optimization. On the other hand, Architectural techniques for power savings include application specific techniques for multi-media hardware systems, and generic techniques like clock gating, on-line profiling based monitoring and control etc. Other paradigms of architectures such as network on chip (NoCs) target power optimization as well. Protocol level power optimization methods include generic techniques employed in wireless standard protocols, as well as techniques specific to multi-media traffic. DPM strategies get increasingly sophisticated due to improved power manageability of hardware components. In this context, there is a positive feedback in action. Power management techniques show the potential for power savings, and this pushes hardware developers to support more advanced (finer grained and lower overhead) power management modes. In this tutorial, we will provide an overview of three main issues in three segments, namely, architecture level, system level and protocol level techniques of power minimization and management, how they influence each other. However, we will not concentrate on low power VLSI techniques.

***Luca Benini** is an associate professor in the Department of Electronics and Computer Science at the University of Bologna. He also holds visiting researcher positions at Stanford University and Hewlett-Packard Laboratories, Palo Alto, California. He is coauthor of the book: Dynamic Power Management, Design Techniques and CAD Tools (Kluwer, 1998) and authored numerous articles.*

***Rajesh Gupta** is the Qualcomm Endowed Chair Professor in the Department of Computer Science and Engineering, UC at San Diego. He is author and/or coauthor of over a hundred articles Prof. Gupta is a recipient of the Chancellor's Fellow at UCI, the National Science Foundation CAREER Award. He is Editor-in-Chief of the IEEE DESIGN AND TEST OF COMPUTERS and serves on the editorial boards of journals.*

***Sandeep Shukla** is an assistant professor in the Department of Electrical and Computer Engineering, Virginia Polytechnic Institute and State University. He also serves as the deputy director of Virginia Tech Center for Embedded Systems for Critical Applications (CESCA). He received 2003 Presidential Early Career Award for Scientists and Engineers and the NSF CAREER Award. He has co-authored and co-edited 3 books, and published almost 80 articles. He is a senior member of IEEE.*