

Tutorial: Physics and Technology: Towards Low-Power DSM Design

Speakers

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The demand for higher functionality and higher performance at lower cost is the main motivation behind the continuous downsizing of CMOS based ICs. The feature size of individual transistor is shrinking from deep sub-micrometer (DSM) to even nanometer region. As the scale of integration improves, more transistors, faster and smaller than their predecessors, are being packed into a chip. This leads to the steady growth of the operating frequency and processing capacity per chip, resulting in increased power dissipation. A need for low-power VLSI chips arises from such evolutionary forces of integration on circuits. The craving for smaller, lighter and more durable electronic products and the increased market demand for portable consumer electronics powered by batteries, translate to low power requirements. Low-power CMOS VLSIs find increasing applications in notebook computers, digital personal communication services having portable multimedia terminals with voice and handwriting recognition facilities. Design of DSM CMOS and its downsizing keeping at the same time power consumption at a manageable level requires deep understanding of the physics involved. The hot carrier effects, velocity saturation and overshoot, impact ionization, DIBL, GIDL, punch through, tunneling effects and hot carrier injection through thin gate play important roles in the design of low power devices and also provide a guideline for further scaling of feature size and control of power level. In addition quantum mechanical effects induce a threshold shift and depth of inversion layer. All the present simulation tools need modification to take into account all the effects. Alternate devices like SiGe HFETs and CMOS on Silicon on Insulator are in the process of evolution. The aim of the tutorial is to cover the basic physics involved in DSM and nanometer sized CMOS ICs, technologies involved and the modeling techniques for low power CMOS and emerging devices.

Professor D. Mukhopadhyay, obtained his M. Tech and Ph. D. degrees from the Institute of Radiophysics and Electronics, University of Calcutta. He joined the Dept. of Electronics and Telecommunication Engineering, Jadavpur University, as a Lecturer in 1969. During the period

from 1975 to 1977, he had been an Assistant Professor in the Dept. of Electrical Engineering, Indian Institute of Technology, Madras. He re-joined Jadavpur University in 1977 where he became a Professor in 1983. Professor Mukhopadhyay specializes in semiconductor materials and devices. He has worked on the high electric-field conduction in compound semiconductors. At Jadavpur University, apart from his teaching and research activities, he had been the principal investigator and co-coordinator in a number of funded projects on ASIC Design, IC Fabrication, Simulation and Modeling of Semiconductor Devices etc. In recent years, Prof. Mukhopadhyay shifted his attention to the Computer Aided Design of Integrated Circuits. With assistance from AICTE and Industries, he set up an Electronic Design Automation (EDA) Laboratory and trained students in this area of industrial importance. He works as the coordinator of the program on "Special Manpower Training Program on VLSI Design" sponsored by the Ministry of Communication and Information Technology. He has delivered several invited talks on "Physics and Modeling Issues in Submicron MOSFETs" and "Low-power Issues in VLSI Design" at conferences and workshops held at various Universities and IITs. Prof. Mukhopadhyay has published about 35 papers in national and international journals and has presented about 20 papers in various conferences. He is a life member of the Indian Physical Society.

Professor Prasanta Kumar Basu: B.Sc. (Honours in Physics, 1963), B. Tech (1965), M. Tech (1966) and Ph.D. (1971) all in Radio Physics and Electronics, University of Calcutta, joined the Institute of Radio Physics and Electronics as a Lecturer in 1971 where he is currently a Professor and Head of the Department. He spent 1972-73 in Catholic University, Belgium as a postdoctoral fellow, 1977-78 in Wurzburg University, Germany as an Alexander von Humboldt Fellow, and 2001 and 2002 as Visiting Professor at McMaster University, Canada. Prof. Basu did experimental and theoretical work on hot electron transport in n-Si, correctly identifying the scattering mechanisms. He then started work on transport and scattering in quantized Si inversion layers in MOSFETs, and in III-V Quantum Wells. Afterwards he focused on optical processes in nanostructures and optoelectronic device applications. He predicted mobility enhancement in Si/SiGe strained Quantum Wells, subsequently verified experimentally elsewhere. He also worked on Si-based optoelectronics including planar lightwave circuits. Presently he is working on performance modeling of HBTs with SiGe or SiGeC as base and Monte Carlo simulation of hot carrier transport in Ge-rich SiGeC layers. Prof. Basu has more than 100 publications in refereed journals, a large number of conference papers and a book entitled "Theory of Optical Processes in Semiconductors: Bulk and Microstructures" (Clarendon Press, Oxford, 1997, 2003). He serves as referees to APS and IoP journals. He is Fellow of IETE and a Member of IEEE.

Professor V. Ramgopal Rao obtained his M. Tech from IIT Bombay in 1991 and Dr. Ingenieur degree from the Faculty of Electrical Engineering, Universitaet der Bundeswehr Munich, Germany in 1997. His doctoral thesis was on Planar-Doped-Barrier Sub 100 nm Channel Length MOSFETs. He was a DAAD fellow for three years during 1994-1996, and, during 1997-1998, and again in 2001, a visiting scholar with the EE Department, University of California, Los Angeles. He is currently an Associate Professor in the Department of Electrical Engineering, IIT Bombay. Dr. Rao's areas of interest include Physics, Technology and Characterization of Silicon CMOS devices for logic and mixed-signal applications, non-volatile memories, and Bio-MEMS. He has over 130 publications in these areas in refereed international journals and conference proceedings and holds two patents, with three other patents currently pending. Prof. Rao is an Editor for the IEEE Transactions on Electron Devices in the CMOS Devices and Technology area. He is also a distinguished speaker identified by the IEEE Electron Devices Society for offering short courses to the industry. He is currently the Chairman, IEEE AP/ED Bombay Chapter, and was organizing committee chair for the 17th International Conference on VLSI Design. He is also a working group member set up by the Govt. of India on Nanotechnology. Prof. Rao is a Senior Member of IEEE and a Fellow of IETE.