

Tutorial: Compact MOSFET Models for Low Power Analog CMOS Design

Speaker

A. B. Bhattacharyya
Jaypee Institute of Information Technology
A-10, Sec-62, Noida, 201 307 (U.P) INDIA

For Low Power CMOS Analog Design the requirements of modeling MOS Devices are both very demanding and stringent. For low power the devices operate at low voltage and low current. The operating regions of the devices pertain to strong, moderate and weak inversion modes with its characteristics device physics and model parameters. From simulation viewpoint the major concern of model development has been the continuity of current and model parameters in the transition region of these modes of operation. For a compact model for analog design these issues have to be addressed along with the effects of scaling down to submicron level. The tutorial proposes to discuss briefly the following:

- Criteria for compact MOSFET model with reference to Low Power Analog Design.
- Review of two and three terminal MOS capacitor (Definition of Strong, Moderate and Weak Inversion, Threshold Voltage, Capacitance-Voltage Characteristics).
- Long Channel MOSFET's static characteristics and Memelink-Wallinga graphical model.
- EKV (Enz-Krummenacher-Vittoz) MOST model for static drain current in weak, moderate and strong inversion.
- Quasi-Static Small Signal model of long channel MOST as a function of inversion level.
- Non-Quasi Static High frequency small signal model for MOST.
- ACM (Advanced single piece Compact Mosfet model).
- Noise model for MOSFET in different inversion regions.
- Modification of long channel Analytical MOSFET model due to scaling.
- Quantum effect.
- A brief Review of SPICE model parameters as a benchmark.

Prof. Bhattacharyya has researched in CMOS analog design for about last 15 years apart from earlier research in MOS technology and device modeling . Have supervised thirty Ph.D. students and six of them are on low power CMOS analog design. Presently supervising three Ph.D. students in the area of low power CMOS design and compact modeling. Have been involved in the development of low power CMOS hearing aids and ultra low power PACEMAKER building blocks. Have taught extensively device model, Analog CMOS Design at UG and PG level in the universities and delivered lectures for practicing engineers in industries. The speaker was the architect and coordinator of microelectronics program at Indian Institute of Technology Delhi during 1974 to 1997. Presently he is organizing research and academic program on VLSI and Embedded design at Jaypee Institute of Information Technology, Noida.