

Tutorial: SoC Design Methodology: A Practical Approach

Speakers

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Today's deep sub-micron semiconductor technology has enabled large-scale integration of multi-million gates consisting of reusable intellectual property (IP), on-chip memory and user-defined logic on a single chip. The design of such SoC has introduced several challenges in terms of increased design complexity in the areas of functional verification, timing closure, physical design, signal integrity, reliability, manufacturing test and package design. This tutorial will discuss a methodology that is based on the successful design of several digital dominated SoCs such as high-speed low-cost communications Processors, VOP and DSL devices, High performance Audio and Video Processors at Texas Instruments. It will provide a complete breadth of digital chip design techniques. In addition, it will cover some issues related to mixed-signal SoC and hierarchical design. Design tradeoffs will be discussed to handle the SoC complexity, and yet meet the time-to-market demands. We will review different methodologies that are followed in the industry to design these chips. Following topics will be covered with examples to explain design challenges and the approaches used to address them:

- Design Planning
- Functional Verification
- Design For Test (DFT)
- Synthesis, Floor-planning, and STA
- Design Closure
- Manufacturing Tests
- Future Challenges

Atul Jain has Ph.D. (1994), M.Sc. (1986), and B.E. (1983) degrees. He is managing SoC designs in broadband applications at Texas Instruments, Dallas. He has successfully managed SoC designs in the area of fixed wireless access, voice over packet (VOP), communications processors, and DSL CPE modems. He has published several journal and conference papers in the area of binary and multiple-valued logic VLSI design. He has organized and presented two hands-on tutorials on "Rapid-prototyping of Digital Designs" and a half day tutorial on "SoC Design Methodology". He has also taught several engineering courses at university and technical college levels.

Anindya Saha has M.E. (1996), B. Tech (1993) degrees. In 1996, he joined Texas instruments (India) where he is currently a Member Group of Technical Staff and working for Broadband

Silicon Technology Center. As part of BSTC design team, he has been associated with several chip designs of Communication Processors for Residential Gateway Systems. Presently, he is working as chip architect for SoC designs for DSL CPE modems and is an active participant in improving the design methodology. He has published about 6 external technical conference papers and has filed 3 patents related to his engineering work. He has also presented an invited tutorial on "Introduction to Static Timing analysis" as part of VLSI Design and Test Workshop, 2002.

Jagdish Rao has a B.E degree (1990), and has since been at Texas Instruments (India). Over the past 14 years, Jagdish has worked on several high speed, low-cost DSP devices and ASICs, and successfully led the design methodology and physical implementation of several multi-million, nanometer SoC designs. Prior to this, he was also involved in co-architecting TI's first ASIC standard cell clock distribution system and joint development of standard cell place and route system with a major EDA company. Jagdish has coauthored over 25 publications at various TI internal and external technical conferences and EDA forums. At TI, Jagdish was elected Member Group Technical Staff in 1996 and Senior Member Technical Staff in 2000. He currently leads the Physical Design competency at TI's SoC Design Technology Center and also manages the DSP Physical Design group.