

# Tutorial: Power-aware, reliable microprocessor design

## Speaker

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In this tutorial, we present the foundational principles and methodologies behind the design of power-efficient, reliable microprocessors. The stress is on early-stage (pre-RTL) definition at the micro-architecture level, although relevant details from lower levels of design (e.g. logic, circuits and below) are also covered where appropriate. We first cover the topic of pre-silicon modeling to estimate performance, power, temperature and reliability, in the context of target workloads of interest to the design team. We then delve into the definition of the optimal pipeline depth for a microprocessor: a task that is one of the basic initial decisions faced by the design team. Subsequently, we cover the topic of adaptive micro-architectures: those that are designed to change with variations in the workload, with the goal of maximizing power-performance efficiency, reliability, or both. We address both active (or dynamic) and passive (or static) power in presenting evaluations of various micro-architectural techniques for power management.

*Dr. Pradip Bose is a Research Staff Member and Manager of Power- and Reliability-Aware Microarchitectures, at IBM Thomas J. Watson Research Center, Yorktown Heights, NY. He received his B. Tech. (Hons.) degree in electronics and electrical communication engineering from I.I.T Kharagpur in 1977; and, his M.S. and Ph.D. degrees in electrical and computer engineering from University of Illinois, Urbana-Champaign in 1981 and 1983 respectively. He has been with IBM Research since May 1983. Dr. Bose has been involved in the modeling and design of all IBM POWER-series processors, beginning with the original RS/6000 machine. During 1992-95 he was on assignment at IBM Austin, where he led the performance modeling and analysis group in support of the POWER3 processor project. Dr. Bose spent the 1989-90 academic year on a sabbatical leave, working at Indian Statistical Institute, Calcutta, India. His current research interests are in the areas of computer architecture, low power design and modeling, VLSI CAD and testing. Dr. Bose has extensive experience as a tutorial speaker: he has given recent tutorial and invited talks at all of the major architecture conferences: e.g. ISCA, HPCA, MICRO, ICS, Sigmetrics, and also at ISSCC-2003. He is very active in conference program committees (e.g. ISCA, MICRO, HPCA and many others) and is the current Editor-in-Chief of IEEE Micro magazine. Dr. Bose is a senior member of IEEE.*