

Device Reliability and Failure Mechanisms Related to Gate Dielectrics and Interconnects

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Abstract

As dimensions shrink, the reliability considerations become more trivial. In deep sub-micron devices, at certain stages of processing, even an atomic layer variation can be a defect. Studies on the physical failure mechanisms in sub-micron devices reveals that the major reliability concerns are the same as that poses before scaling. A comprehensive overview on the reliability issues in ultra thin gate dielectrics and copper interconnect material is given to link how the physical effects on devices can be a threat to long-term reliability.

1. Introduction

The feature size reduction in devices paves the way for the reduction in electrical defect density also, even though the process complexity increases. On the technology point of view, this trend means a lot in terms of contributions from design to process and device engineering. This has not only led to the vast knowledge base in device engineering, but has resulted in extensive studies on the physics of materials and interfaces [1].

Understanding and enhancing the reliability of devices needs detailed

physical analysis to study the failure mechanisms irrespective of the technology. However, such studies have become a more interactive process between design, process and device engineering, and this paper deals with the intricacies in the study of ultrathin gate oxides and its behaviour in sub-micron devices, as well as issues related to copper metallization. An overview of various studies in this area is presented here as an extended abstract. Discussions on the device related failure issues due to ultrathin gate oxide breakdown and electro-migration reliability of copper metallization are presented from a device physics point of view.

2. Gate Dielectrics Reliability

The reliability of ultrathin gate oxide (Gox) has been a major concern for the scalability of metal oxide semiconductor (MOS) devices. The properties of silicon dioxide have been projected to limit the scaling of CMOS technology in different ways [2-4]. Different physical models of the reliability of ultrathin gate oxide have been proposed [5-9]. Eventhough, numerous efforts have been made in the studies of thin gate oxides (<6nm), a number of important issues have still

wide gap between the results and the models projected [10].

Several models such as impact ionization, anode-hole injection, field enhanced bond breakage, etc have been studied in detail, but without clear consensus in arriving a unique method due to lack of clear understanding of the microscopic failure mechanisms involved in the breakdown [11]. However, the trap assisted geometric breakdown formulation by the percolation model [12] has been found consistent with experimental statistics. Recently, microscopic failure mechanism study of devices using ultra thin gate oxides has shown that the nature of failure does not limit to the gate oxide alone, but affect the entire region [13-15]. Details of those analyses, which provide certain new information on device reliability issues are briefly discussed.

Physical analysis of n/p MOSFET devices using ultrathin gate oxides of thicknesses ranging from 16Å to 40Å, after oxide breakdown stressing depict physical damage at the gate oxide region. It has been shown that the degradation is not only an electrical breakdown phenomenon, but physical damage also happens to the structure, in both the cases of soft breakdown (SBD) as well as hard breakdown (HBD) failures [13,14]. Depending on the stress levels, the physical damage extends from very localized epitaxial growth at the interface (Dielectric Breakdown Induced Epitaxy – DBIE) to complete rupture of oxide and heavy damage to gate region and substrate. The physical mechanism of the formation of DBIE is related to the dynamic percolation process, where by the DBIE forms as a dynamic evolution. This growth can result in HBD of the gate dielectric. As the gate oxide thickness

reduces to its physical limit, SBD, DBIE and HBD are found to converge and that can be correlated to the percolation conduction as well. This epitaxial growth phenomenon is found to be polarity dependent [16].

Another physical mechanism observed during the gate dielectric breakdown in the small MOS device structures is the stressed migration of salicides from the gate as well as underneath the spacer region. This phenomenon, known as dielectric breakdown induced metal migration (DBIM), [15] can initially result in the increase in leakage current. Under constant voltage stress, the ultrathin gate oxide breakdown comprises of sequential events involving SBD, DBIE and HBD [17]. The physical phenomenon of this type degradation in the device structure is a resultant of the scaling and the thermal effects associated with the electrical breakdown [18, 19]. An overall picture of physical and electrical degradation in very thin gate dielectrics can be summarized as in Table 1.

Table 1 : Electrical and Physical Degradation due to G_{ox} stress

<i>Electrical</i>	<i>Physical</i>	
I_g increase G_m degradation		SBD
I-V degrade G_m degradation	Epi formation Si defects	SBD + Epi growth
I_g shoots up Transistor fails	G_{ox} rupture and epi grow	HBD

In the initial stage of SBD, the characteristics degrade, but the device will be functional. However, the degradation implies that microstructural damage at the gate region has already been initiated in the transistor. Such a situation of the functional device is a serious threat to device reliability. Figure 1 shows an

experimentally observed convergence of gate oxide thickness for stress degradation.

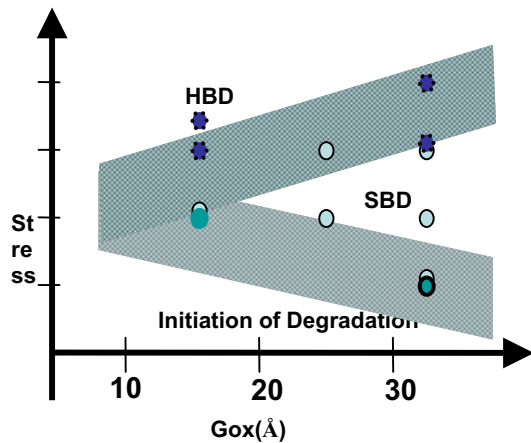


Figure 1 : A convergence in gate oxide thickness to effect the degradation at different stress level (ref : 17).

At gate oxide thicknesses less than 10\AA , the device may fail instantaneous at any stage of stress, and is a point of concern in scaling.

3. Cu Interconnects Reliability

As new interconnect materials emerge, the issues related to its functioning and reliability also become critical. Copper, even though is a good electromigration (EM) resistant material, shows very typical failure mechanisms in device. With multi-layer Cu metallisation having different types of interlayer dielectrics (ILD), the issues of interfaces and adhesion become critical. Cu damascene layers show abrupt failures depending on the direction of current flow. This coupled with effect of various low-k materials as inter-layer dielectrics (ILD) make the issues critical not only for processing, but for design as well. A brief overview of the Cu electromigration behaviour with silicon oxide / nitride as well as low-k materials as ILD is presented here.

Cu dual-damascene structures with oxide ILD and nitride interfaces revealed multi-mode failures which are dominated by void formation at via bottom interface [20]. In multi-level metal structures, the asymmetry in the failure times is observed and is found to be the result of difference in the location of void formation and growth. The interfacial properties of Cu / Si_3N_4 interface cause such asymmetry [21]. Figure 2 shows an asymmetric mean time to failure (MTTF) behavior of two layers of Cu damascene structures using SiO_2 as ILD and Si_3N_4 as barrier layer. As such, asymmetric via reliability is an intrinsic characteristic of the Cu interconnect technology.

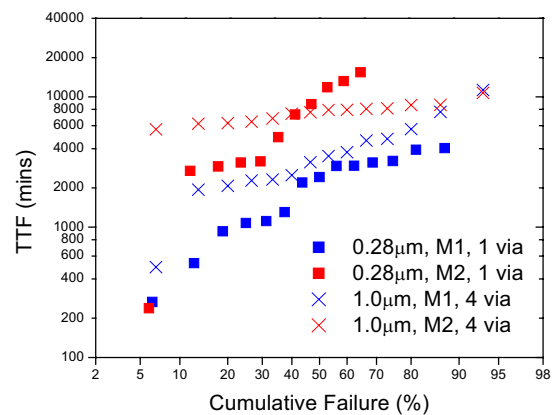


Figure 2 : Asymmetric nature in MTTF for Cu dual damascene structures (ref : 21).

Further, the Cu grain size as well as the resistance variation with annealing plays an important role in EM reliability. For high aspect ratio metal lines, high temperature anneal has got a greater impact [22]. Also, at re-crystallization the sheet resistance of copper drops. The texture development has got influence on anneal conditions. To minimize the stress, the anneal temperature has to be reduced, but the grain structure development is at elevated temperature. This projects the

need of a trade off in processing in view of greater reliability.

Cu/low-k structures show different types of failures compared with Cu/oxide ILD. The integration of low-k as ILD found to degrade electromigration performance and induces new failure mechanisms [23]. Compared with oxide, low-k dielectrics are softer, poor thermal conductor and have more elastic nature. As the thermo-mechanical properties are of importance for electromigration reliability, the full impact of Cu/low-k in long-term reliability is yet to be understood.

A brief overview of the scaling effects of gate dielectrics as well as the introduction of copper interconnects in device reliability has been discussed in this extended abstract.

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5. References

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