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High Speed Integrated A to D Converters

Abstract

Flash converters achieve A to D conversion in a single clock-cycle. They are fast devices by essence but area and power consumption increase exponentially with numbers of bits. Nine to ten-bit converters require large transistor sizes in order to cope with narrow offset tolerances of the comparators. A 1 mm² 10-bit CMOS converter with a sample rate of 50 MS/s and 240 mW power consumption has been reported. The converter takes advantage of offset averaging techniques to keep transistor sizes minimal.

Five to six-bit resolution full-flash converters are more customary. Multistep converters take advantage of low-resolution flash devices. They require however one Op Amp as opposed to full-flash converters, which don't. Consequently, their sampling rates reach typically a few ten to hundred MS/s at most. Multistep converters mingle a coarse low-resolution N-bit flash converter with a concurrent equal resolution D to A parallel converter to generate the analog coarse N-bit approximation of the input signal. This signal is subtracted from the analog input to generate coarse quantization noise, which undergoes one or more subsequent conversion steps. The data generated during every step are concatenated in order to produce the actual output words. Pipelining is contemplated generally in order to compensate for the larger conversion times but at the expense of latency of course. Several identical converters may be put to work in a time-skewed architecture in order to further increase sampling rates.

A class of fast devices that outperforms the previous ones as far as speed but without reaching the performances of full-flash converters is known currently as folding converters. The evaluation of coarse data results from the comparison of the unknown analog input to a folded reference, which mimics the above A to D to A conversion in the analog domain. Since no Op Amp is needed, fast decisions can be made. The number of comparators is smaller than with full-flash devices thanks to interpolation techniques.

The presentation will review examples of the above converters and illustrate recent developments. The impact of circuit tolerances, mismatches etc. upon converter's performances will be considered in detail. Measures to reduce the impact of impairments will be described concurrently.