

## Tutorial 7

### Embedded Test for Low Cost Manufacturing

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#### Abstract

The transition to sub-nanometer designs demands new requirements in digital circuit testing. As we move to smaller geometries – new defects that are not detected by conventional stuck-at pattern test sets are surfacing. Stuck-at pattern test was good in detecting gate-oxide defects, but is ineffective in detecting defects that are predominantly in routing, such as metal bridges or in-line resistive changes (open/plugged vias). In order to improve the overall test quality, additional test vectors are necessary to either target the routing defects using existing fault models such as transition and path-delay faults, or new fault models need to be developed to abstract the behavior of such defects that are increasingly showing up in smaller geometries. Numerous studies have shown that a good test set should contain vectors that detect a variety of fault models as every one of them uniquely detects certain defects that would otherwise escape the manufacturing test process.

As discussed in the previous paragraph, the quality of the manufactured parts could be improved by increasing the size of test vector set. However, the rapid growth in the complexity of circuits have resulted in an explosion in the number of scan vectors that are usually required to just target

stuck-at faults. Since the data memory in current Automatic Test Equipment (ATE) is limited, either the test sets need to be truncated or the ATE memory has to be re-loaded multiple times so that the test data could be applied in phases. Truncation of test set results in degrading test quality in an unpredictable way as the fault coverage deteriorates. On the other hand, re-loading ATE memory is very expensive as the time taken to do one re-load is often more than the time taken to apply the test set to the device-under-test (DUT). In addition, as test data increases, the test application time increases proportionately since each and every test vector has to be shifted in and out of the circuit via scan chains formed by connecting all the sequential elements in a circuit. As tester time (amount of time a DUT spends in the ATE) is quite expensive, test data volume, therefore, directly contributes to increasing test cost. The problem of increasing test data volume is further aggravated when additional fault models such as delay and bridging defects are targeted. Experimental results show that a test set size usually tends to increase 3-5 times when just transition vectors are added.

Rising test cost and improving the test quality are indeed the biggest challenges as we move towards sub-nanometer designs. This tutorial will present state-of-the-art embedded test technology, practices, and automation tools for high-quality low cost manufacturing test. We will start by introducing the test requirements to manufacture high quality devices, explain the factors contributing to increasing test costs, and introduce the pros and cons of non-embedded versus embedded test techniques. We will next focus on embedded test structures and compare pseudo-random versus deterministic forms of embedded tests. In the process, guidelines for design of BIST-able cores, techniques for random pattern testability, as well as BIST structures for random logic and memory arrays will be covered. The rising test costs mainly driven by increasing circuit complexity and demand for higher test quality is being addressed today by incorporating hardware based compression techniques for scan data. The tutorial will cover new embedded test methodologies based on deterministic patterns, such as LFSR reseeding, OPMISR, Smart BIST, and Embedded Deterministic Test. Test quality will be addressed by putting special emphasis on at-speed tests. The tutorial will also cover numerous applications and case studies to illustrate the concepts. The attendees will also receive hard copies of the presented material.

## Biography

Janusz Rajski received the M.Eng. degree in electrical engineering from the University of Gdansk, Poland, in 1973, and the Ph.D. degree in engineering from the Technical University of Poznan, Poznan, Poland, in 1982. From 1973 to 1984, he was a member of the faculty of the Technical University Poznan. In June 1984, he joined McGill University, Montreal, Canada, from 1989 he was an Associate Professor. In 1995 he joined Mentor Corporation, Wilsonville, Oregon, where he continues his work as Chief Scientist heading a CAD research group. His main research interests include design automation and testing of VLSI, design for testability (DFT), Embedded Test, and logic synthesis. He has published more than 100 research papers and is a co-inventor of several patents in these areas. He is a co-author of a book on BIST published by Prentice Hall. He was a co-recipient of the 1993 Best Paper Award for the paper on synthesis of testable circuits published in the IEEE Transactions on Computer-Aided of Integrated Circuits and Systems. He is also a co-recipient of a Best Paper Awards for a paper published at European Design and Test Conference, two Best Paper Awards for papers published at the VLSI Test

Symposium, and one Honorable Mention Paper published at the International Test Conference. Rajski was a Guest Co-editor of the June 1990 and January 1992 Special of the IEEE Transactions on Computer-Aided Design of Integrated Circuits Systems devoted to the 1987 and 1989 International Test Conference. He is a member of the editorial board of IEEE Transactions on Computers, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Journal of Electronic Testing (JETTA) and an associate editor for the IEEE Design and Test of Computers Magazine. He has served on technical program committees of various conferences including Asian Test Symposium, European Design and Test Conference, International Test Conference, Design Automation Conference, International Conference on Computer-Aided Design, and VLSI Test Symposium. He is a co-founder and the General Chair of the International Test Synthesis Workshop. Dr. Rajski has given presentations at all major international conferences in the area of testing.

Nilanjan Mukherjee received a B.Tech. (Hons) degree in Electronics and Electrical Communication Engineering from Indian Institute of Technology, Kharagpur, India, and a Ph.D. degree from McGill University, Montreal Canada. He is presently an Engineering Manager in the Design, Verification and Test division at Mentor Graphics. His primary interests are focused on developing next generation test methodologies for DSM designs, test synthesis, test compression, memory test, and fault diagnosis. Prior to joining Mentor Graphics, Dr. Mukherjee worked at Lucent Bell Laboratories in Princeton, New Jersey, where he primarily contributed in the areas of Logic BIST, RTL testability analysis, path-delay testing, and on-line testing. He has co-authored more than 30 technical articles in leading IEEE journals and conferences. He was an invited author for the special issue of IEEE Communications Magazine, June 1999. He is also a co-inventor for 9 US patents. Nilanjan was the recipient of the Best Paper Award at the 1995 VLSI Test Symposium. He co-authored a paper that received the Best Student Paper Award at the Asian Test Symposium in November 2001. Dr. Mukherjee has reviewed papers for numerous IEEE journals and conferences. He also served as a member of the technical program committee for DDECS 2003. Nilanjan has given invited talks at numerous companies and universities in USA and India. He also delivered tutorials on DFT at major international conferences and delivered DFT seminars organized by Mentor Graphics at various locations in USA and India.