Tutorial 6

Bridging the Gap between Asynchronous Design and Designers

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Abstract

Asynchronous circuits are promising to tackle problems such as electro-magnetic interference, power consumption, performance, and modularity of digital circuits. The goal of this tutorial is to introduce state-of-the-art tools and methodologies for their design. It will cover aspects such as specification, architectural design and controller synthesis tools, of asynchronous circuits. The tutorial will concentrate on a particular design methodology for control circuits based on specifications with Signal Transition Graphs. It will also cover strategies for the design of complex circuits with different clock domains (GALS: globally asynchronous locally synchronous) and de-synchronization of synchronous circuits. Finally, some succesful stories from industrial designs will be presented. The tutorial is organized in five parts.

1. Basic concepts of asynchronous circuits.

Synchronous vs. asynchronous: differences in design, synthesis, verification and testing. Asynchronous communication with handshake protocols. Micropipelines and other design styles. Some building blocks: asynchronous latches. Specification and implementation of control circuits. Delay models and classes of asynchronous circuits. Template-based asynchronous design.

2-D integrated pipelining.

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2. Logic synthesis from concurrent specifications.
Specification models: Signals Transition Graphs (STGs), Burst-mode FMSs, CSP. Design flow for the synthesis from STGs. Derivation of the state graph and next-state functions. State encoding. Implementability conditions for hazard-free circuits. Synthesis of speed-independent circuits.

3. Synchronization of complex systems.
The problem of synchronization with multiple clock domains. Metastability and the mutual exclusion element (MUTEX). Design of arbiters.Globally asynchronous locally synchronous (GALS) systems: schemes with pausable clocks and STARI.

4. Design automation for asynchronous circuits.

- Integration of the asynchronous methodology with state-of-art commercial EDA tools. End of deterministic design: process and environment variability. Probabilistic parameter distributions (power, delay). Advantages and limitations of the statistical approach.
- De-synchronization: a new paradigm for a direct synthesis of asynchronous circuits using synchronous reasoning. Interfacing de-synchronized circuits with a synchronous environment.
- Quasi-delay insensitive automated design: synthesis of asynchronous circuits from synchronous RTL using local timing assumptions. Examples of the NCL and phased logic methodologies.

5. Industrial experiences.
This part will first provide an overview of the semi-automated asynchronous design flow used at Fulcrum Microsystems that enable close to full-custom performance with far less effort than typical full-custom flows. It will then overview several of the chip designs that Fulcrum has developed, including a high-performance SoC crossbar that is the Nexus of their solution to globally asynchronous locally synchronous designs and PivotPoint their first commercial product that uses this Nexus surrounded by 6 SPI-4 v.2 input/output interfaces, forming a 6-port SPI-4 switch chip.

Biography

Peter A. Beerel received the B.S.E. degree in electrical engineering from Princeton University, Princeton, NJ, in 1989, and the M.S. and Ph.D. degrees in electrical engineering from Stanford University, Stanford, CA, in 1991 and 1994, respectively. He is the Vice-President of Asynchronous CAD and Verification at Fulcrum Microsystems, a startup company developing and commercializing asynchronous designs. He is also Associate Professor, currently on leave, from the Department of Electrical Engineering-Systems at University of Southern California (USC), Los Angeles.

He has consulted for Yuni Networks and AMCC in the areas of networking chip design, Intel and Asynchronous Digital Design in the areas of asynchronous design and CAD, and

TrellisWare Technologies in the area of communication chip design. Dr. Beerel was a recipient of an Outstanding Teaching Award in 1997 and the Junior Research Award in 1998, both from USC's School of Engineering. He received a National Science Foundation (NSF) Career Award and a 1995 Zumberge Fellowship. He was also co-winner of the Charles E. Molnar Award for two papers published in ASYNC'97 that best bridged theory and practice of asynchronous system design and was a co-recipient of the best paper award in ASYNC'99. Dr. Beerel is co-author of five patents in the area of asynchronous circuits and CAD. He was a Member of the Technical Program Committee for the International Symposium on Advanced Research in Asynchronous Circuits and Systems from 1997-2003 and was Program Co-chair for ASYNC'98. He has served on the Technical Program Committee for ICCAD'00, ICCAD'01, and ICCAD'02.

His currently research at USC targets high-speed asynchronous circuit design and verification, focusing on performance optimization, high-speed circuit design, and timing verification. At Fulcrum Microsystems, he leads a CAD team responsible for the high-level design tools and a verification team responsible for system-level verification.

Jordi Cortadella received the M.S. and Ph.D. degrees in Computer Science from the Universitat Politecnica de Catalunya, Barcelona, Spain, in 1985 and 1987 respectively. He is a Professor at the Department of Software of the Universitat Politecnica de Catalunya. In 1988, he was a Visiting Scholar at the University of California, Berkeley. His research interests include computer-aided design of VLSI systems with special emphasis on synthesis and verification of asynchronous circuits, concurrent systems and HW/SW co-design. He has coauthored over 100 research papers in technical journals and conferences. He has served on the technical committees of several international conferences in the field of Design Automation and Concurrent Systems. He was the Symposium Co-Chair of the 5th International Symposium on Advanced Research in Asynchronous Circuits and Systems in Barcelona, 1999. He is co-organizer of ETAPS 2004 and PC co-chair of the Int. Conf. on Application and Theory of Petri nets 2004. He is the main author of the tool petrify, currently used by several industries and Universities for the synthesis of asynchronous control circuits.

Alex Kondratyev received the M.S and Ph.D. degrees in computer science from the Electrotechnical University of St.Petersburg, Russia in 1983 and 1987, respectively. He is currently a research scientist in Cadence Berkeley Laboratory. In 2000 he took a position of senior scientist in Theseus Logic. Before that from 1993 to 1999 he was Associate professor of the Hardware Department at the University of Aizu. From 1988 to 1993 he was with the R&D Coop TRASSA, St.Petersburg, Russia. Previously, he held a position of assistant professor in the Electrotechnical University of St.Petersburg. He is a coauthor of two monographs on asynchronous methodology and has published more than 70 papers in technical journals and conferences. Dr. Kondratyev was a co-chair of Async'96 Symposium, co-chair of CSD'98 Conference and has served as a member of the program committee for several conferences.

His research interests include several aspects of the computer-aided design with particular emphasis on asynchronous design and theory of concurrency.