

## Tutorial 3

### High Level Design Validation: Current Practices and Future Directions

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#### **Abstract**

With the increasing complexity of VLSI design and time-to-market pressures, two major paradigms have emerged to address the difficulties currently being faced by the industry. They are: (1) the use of higher levels of design abstraction and (2) efficient and seamless design reuse. The design and modeling of a chip at higher levels of design abstraction brings with it additional burdens of validation, verification and testing at these levels.

This tutorial will discuss current industrial practices and academic research in design verification and validation at these levels—specifically RTL, behavioral, specification and system level. High level modeling using languages like UML and Esterel will be presented and the associated verification challenges highlighted. Verification engines on higher order logic like theorem proving and decision procedures will be discussed. The tutorial will touch upon mapping, abstraction and refinement techniques used to make traditional formal verification techniques such as model checking applicable at the specification level, using languages like C, SystemC, SpecC and System Verilog. Several difficult problems of sequential circuit equivalence checking, timed vs untimed model equivalence checking, and concurrent vs sequential design

equivalence checking will be highlighted. Open research issues and current solutions will be discussed.

The next part of the tutorial will discuss formal and semi-formal verification techniques that have traditionally been applied to FSM models but are also potentially applicable to verification problems at higher level of abstraction and to SoC verification. The current capabilities and limitations of these techniques will be discussed along with EDA vendor tool offerings in these areas. Industrial practices and recent research results in property-based model checking will be presented. Subsequently the tutorial will focus on semi-formal methods like bounded model checking, symbolic trajectory evaluation, and symbolic simulation. In bounded model checking recent advances in SAT and ATPG based procedures will be presented. Finally simulation based validation methods will be covered. HDL coverage analysis techniques and current advances in interface protocol checking using transition coverage will be presented. Simulation based assertion checking methods will be discussed. The tutorial will focus on automatic test bench generation based on test bench automation languages like Sugar etc. It will elaborate on high level ATPG techniques and how they can be used to automatically generate validation vectors. An industrial design verification experience will be presented in the formal and the simulation based arena to show the application of these techniques from an industrial perspective. Lastly, issues and problems peculiar to SoC verification will be discussed.

The tutorial will conclude by presenting some future research directions and industrial trends in verification and validation of higher level models in the VLSI design process.

## **Biography**

Indradeep Ghosh received the B. Tech. degree in Computer Science and Engineering from the Indian Institute of Technology, Kharagpur, in 1993, and the M.A. and Ph.D. degrees in Electrical Engineering from Princeton University, in 1995 and 1998, respectively. Since 1998 he has been a member of research staff in the Advanced CAD Research group at Fujitsu Laboratories of America in California. He has co-authored more than 30 technical articles in international journals and conferences and holds 2 US patents. His work has received an Honorable Mention Award at the International Conference on VLSI Design (1998). His research interests include ATPG, design for testability, built-in self-test, validation and verification at the register transfer level and higher levels of abstraction. In Fujitsu he has been involved in design verification of real industrial designs.

Mukul Prasad received the B.Tech. degree in Electrical Engineering from the Indian Institute of Technology, Delhi, in 1995, and the Ph.D. degree in Electrical Engineering & Computer Sciences from the University of California, Berkeley in 2001. Since 2001 he has been a member of the research staff in the Advanced CAD Research group at Fujitsu Laboratories of America in California. His doctoral thesis and subsequent research has involved the development and application of verification technologies such as Satisfiability solvers. He has authored and presented several papers in international conferences and journals on this topic. His work has received a Best Paper Award at the Design Automation & Test in Europe Conference, 2002. His current research addresses various problems in system-level design validation.

Rajarshi Mukherjee received the B.Tech. degree in Electronics and Electrical Communication Engineering from the Indian Institute of Technology, Kharagpur in 1991, the M.S. degree in Computer Science from Texas A&M University in 1994, and Ph.D. degree in Computer Engineering from the University of Texas, Austin in 1996. From 1996 to 2003 he was with the Advanced CAD Research Group at the Fujitsu Laboratories of America where he carried out research and development in various aspects of verification and diagnosis of digital systems. He has co-authored more than 20 papers in international conferences and journals and holds 5 U.S. patents in these areas. He also worked as a verification engineer on several design projects at HAL Computer Systems and at Fujitsu Labs. Currently he is with Calypto Design Systems in Santa Clara, California, working on developing next generation EDA tools for verification and synthesis.

Masahiro Fujita received his Ph.D. degree in Engineering from the University of Tokyo in 1985 and shortly after joined Fujitsu Laboratories Ltd. From 1993 to 2000 he had been assigned to Fujitsu's US research office and directed the CAD research group. In March 2000, he joined the department of Electronic Engineering in the University of Tokyo as a professor. He has written over 100 technical papers on all aspects of logic design CAD. He has received several awards from Japanese major scientific societies on his works in formal verification and logic synthesis. His doctoral degree thesis was written in early 80's and on model checking. Since then he has been involved in many research projects on various aspects of formal verification. Professor Fujita is the chair of the SpecC Language Specification Group.