

Tutorial 2

Physical Design Trends and Layout-based Fault Modeling

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Abstract

Semiconductor industry has been driven by Moore's law for almost a quarter century. Device size miniaturization has allowed dense packing of transistors while the improved transistor performance has led to significant increase in frequency. Physical design of integrated circuits has always faced new challenges posed by emerging technologies. Performance requirements and high yield being related to physical design, a two-pronged approach from the design as well as the test platforms is mandated. This tutorial aims at presenting the concerns and techniques that are significant to both the circuit designers and developers of CAD tools for physical design and layout-based fault modeling and extraction. First, current technology trends in VLSI with

their impact on the design flow in general and physical design in particular are introduced. Next, the challenging issues in partitioning, floorplanning and placement, and routing are presented. Salient methods and representations are discussed. Then, recent topics in deep sub-micron (DSM) regime such as interconnect planning and synthesis, which involve interconnect architecture design, delay estimation, delay reduction by buffer insertion, wire sizing are addressed. The pertinent problem of clock skew management in clock-tree synthesis is discussed. Post-placement logic rewiring techniques for further optimization of delay, power, reliability are described. Among the grand challenges posed in ITRS 2002, layout design problems arising in state-of-the-art mask lithography and manufacturability take the lead. Of these, a glimpse of optimal proximity correction of the mask and phase shift masking for enhancing sharpness is given. Algorithms for dummy fill synthesis to achieve uniform density preferred for chemical-mechanical polishing are covered. The issues of formatting and compacting the enhanced layout data are also raised. Finally, device scaling has led to blurring of the boundary between design and test and eroded the predictability of test quality based on classical stuck-at fault coverage. New fault models at the core of test generation to overcome the test quality crisis are described. Extraction of such faults requires analysis of the design at the physical and circuit levels of abstraction while considering failure modes observed during manufacturing. An overview of layout analysis methods for extraction and targeting of defect based faults such as bridge and opens, and circuit marginality related failures such as crosstalk, power supply droop is provided.

Biography

Susmita Sur-Kolay received the B.Tech. degree in Electronics and Electrical Communication Engineering from the Indian Institute of Technology, Kharagpur, India in 1980, and was the recipient of President of India Gold medal. She pursued doctoral studies in the Theoretical Computer Science group of Laboratory for Computer Science at the Massachusetts Institute of Technology, USA where her research in graph algorithms with applications to algorithmic VLSI physical design began. Since 1987, she has been in the Advanced Computing and Microelectronics Unit of Indian Statistical Institute, Kolkata, India where she is presently an Associate Professor. From 1993 to 1999, she was a Reader in the Department of Computer Science and Engineering of Jadavpur University, Kolkata, India. She has authored or co-authored over 30 papers, served on the Program Committees of several Conferences on VLSI Design and algorithm design, and collaborated on sponsored research projects. Her research interests are in combinatorial algorithms and algorithmic CAD for layout design and fault simulation.

Parthasarathi Dasgupta is presently an Associate Professor in the Management Information Sciences group at the Indian Institute of Management Calcutta. He received the B.Tech. degree in radiophysics and electronics, M.Tech. and Ph.D. degrees in Computer Science all from the University of Calcutta in 1983, 1985, and 1997, respectively. In 2001-2002, he visited the Dept. of Computer Science and Engineering at the University of California, San Diego. He has also taught at the Department of Computer Science & Engineering, Jadavpur University, and ACM Unit, Indian Statistical Institute. He has published several papers in journals and international conference proceedings. His research interests are in VLSI CAD, AI, and analysis of algorithms.

Bhargab B. Bhattacharya received the B.Sc. degree in physics from the Presidency College, Calcutta, India, the B.Tech. and M.Tech. degrees in radiophysics and electronics, and the Ph.D. degree in computer science all from the University of Calcutta. Since 1982, he has been on the faculty of the Indian Statistical Institute, Calcutta, where he became full professor in 1991. As Visiting Professor, he had been with the Department of Computer Science and Engineering, University of Nebraska-Lincoln, during 1985-1987, and 2001-2002. He also visited the Fault-Tolerant Computing Group, Institute of Informatics at the University of Potsdam, Germany, as Guest Professor during 1998-2000. His research interest includes logic synthesis and testing, physical design of VLSI circuits, computational geometry, and image processing architectures. He has published more than 120 papers in archival journals and refereed conference proceedings. He had collaboration with Intel Corporation, USA and IRISA, France, for development of image processing hardware and reconfigurable parallel computing tools. Dr. Bhattacharya is a Fellow of the Indian National Academy of Engineering. He served on the conference committees of the International Test Conference (ITC), the Asian Test Symposium (ATS), the VLSI Design and Test Workshop (VDATE), the International Conference on Advanced Computing (ADCOMP), and the International Conference on High-Performance Computing (HiPC). For the International Conference on VLSI Design, he served as Tutorial Co-Chair in 1994, as Program Co-Chair in 1997, and as General Co-Chair in 2000.

Sujit T. Zachariah completed his undergraduate degree in Electronics and Communication Engineering from the University of Kerala (India), and was the recipient of the gold medal. He holds two Master's degrees, one in Computer Science and another in Electrical Engineering, and the PhD degree in Computer Science, all from the State University of New York. He has been with the Intel Corporation since 1998 and currently manages the Design/Test Technology group at Intel India Development Center, Bangalore. He has authored (or co-authored) fifteen papers in leading international VLSI CAD conferences/journals and holds three patents. He also spends part of his time mentoring VLSI test CAD research at the Indian Institute of Technology, Chennai, and at the Indian Statistical Institute, Kolkata.