Tutorial 1

Technology CAD: Technology Modeling, Device Design and Simulation

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Abstract

In the semiconductor industry, device densities have grown exponentially in the last three decades. With each new generation of integrated circuit (IC) manufacturing technology, the complexities of IC fabrication processes and devices are increasing significantly. Thus, the intuitive analysis of device characteristics using first-order assumptions about the physical effects and impurity distributions within the semiconductor devices is no longer adequate to develop an advanced IC fabrication technology and devices. As a result, technology CAD (TCAD) that accurately predicts the process and device characteristics of anticipated wafer fabrication technology is indispensable for future IC fabrication technology and device development. TCAD is crucial in quantifying potential roadblocks, indicating new solutions, and offering continuous scaling of silicon technology to its fundamental limits. Presently, TCAD is challenged by a number of fundamental problems such as accuracy, predictability, and inadequate physics such as microscopic diffusion mechanisms, quantum mechanical transport, molecular dynamics, quantum chemistry, and so on. This tutorial provides a detailed survey of the challenging issues of TCAD in technology and device design, insight into the foundation of TCAD tools, calibration of physical models for predictive bulk-process and device simulations, and practical examples form the industrial usage of TCAD in research and development. The tutorial is organized in four lectures. The first two lectures are intended to provide the foundations of bulk-process and device TCAD and the last two lectures are devoted to industrial application of TCAD with practical examples.

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The tutorial begins with a general overview of TCAD and the limitations and challenges of process and device TCAD for IC fabrication process and device engineering. The first lecture introduces the physical models such as ion implantation, implant damage, diffusion, point defects, oxidation, and so on implemented in process TCAD point-tools for bulk-process modeling and simulation. This session, also, highlights the limitations and challenges of physical models and numerical methods.

The second lecture covers the physical models implemented in device TCAD tools for numerical modeling of IC devices with special emphasis on emerging topics like quantum mechanical confinement, tunneling, and discrete dopant effects in nano-scale devices. Examples are used to show the usage and limitations of drift-diffusion as well as hydrodynamic models in nano-scale device simulation. The third lecture is devoted to the industrial usage of TCAD for predictive process and device simulation. The critical issues covered in this session are physical model calibration, selection of effective physical models, numerical aspects, grid generation, and so on. The general philosophy and the step by step procedure of numerical model calibration for predictive application of TCAD in technology and device design are presented. The practical examples are used to show that the well-calibrated TCAD tools can be efficiently used for next generation IC fabrication technology and device development. The final lecture covers the application of TCAD in device research. Step by step procedure to design simulation structures, perform simulation, and analyze simulation results is described. The simulation examples such as sub-100 nm CMOS devices, FinFETs, bipolar junction transistors, flash memory cells etc. are discussed.

Biography

Dr. Samar Saha is currently the manager of Technology Simulation group at Silicon Storage Technology, Inc., Sunnyvale, CA, USA. He is, also, an Associate Graduate Faculty in Electrical Engineering (EE) department at the University of Nevada, Las Vegas, USA and an Adjunct Professor in EE department at Santa Clara University, Santa Clara, CA, USA. Since 1984, Dr. Saha worked at National Semiconductor, LSI Logic, Texas Instruments, and Philips Semiconductors. Prior to working in industry, he worked as an Assistant Professor in EE department at Southern Illinois University, Carbondale, IL and in EE department at Auburn University, Auburn, AL. His research interests include process and device modeling of silicon nanotransistors and nano-CMOS technology, sub-100 nm CMOS process and device architecture, quantum and hot-carrier effects in deep sub-micron devices, development of efficient TCAD application methodologies, and TCAD and R & D management. He has published more than 60 papers and holds four US patents. He received the Ph.D. degree in Physics from Gauhati University, Guwahati, India and the M.S. degree in Engineering Management from Stanford University, Stanford, CA, USA. Dr. Saha is a senior member of IEEE, member of IEEE EDS Compact Modeling Committee, and member of ISQED 2004 technical committee.

Mr. Bhaskar Gadepally is currently an adjunct Professor in the Electrical Engineering department at IIT Bombay and Chairman of Reliance Software Consulting Inc. of Campbell,

California. Mr. Gadepally's career has spanned management and individual contributor roles at Motorola, National Semiconductor Corp., and AT&T Bell Labs. The two decades plus of his career has been in the development and deployment of modeling and simulation capabilities for VLSI design and technology development. His interests include strategy setting for advanced modeling & simulation and technology transfer from "research to critical path acceptance." Mr. Gadepally holds several patents, has published in research journals, and has presented at international conferences. He served as the first co-chair of the Compact Modeling Council. He holds an M.S. from the University of Florida, Gainesville, USA and a Bachelor of Engineering from M. S. University, Baroda, India.