

# Definition, Design & Development of the IXE2424 Network Switch/Router ASIC

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## Abstract

This paper highlights key aspects of the cumulative technical experience of the past two years at Intel, Bangalore, in defining, designing, implementing and ramping to production of the Intel IXE2424 ASIC. The IXE2424 is a Layer 2-3-4 Network Switch/Router, consisting of over twenty-five million transistors, manufactured in 0.18u 1P6M CMOS process. The team at Bangalore completed all steps of front end and backend design, taped out the product, debugged first silicon and finally taped out a production-worthy revision.

The paper starts with what happened at Project Kickoff in defining the ASIC as a part of a system solution for market requirements, how technology selection was done, how chip complexity and chip/board cost was estimated, and how development resources and schedule were estimated.

The body of the talk dwells on aspects of the sequential front end steps in designing the ASIC - Architecture, micro-architecture, usage of IP cores, RTL coding, Design for test, validation, synthesis and timing analysis. It then talks about the Backend steps of Floorplanning, Clock Tree Synthesis, Place & Route, Parasitic Extraction, ECOs, Backend Verification and the tapeout flow.

However, rather than attempting to describe a chronological history of the design and development effort, this paper will focus on the unique challenges faced at each of the above stages of definition, design, implementation – and how such challenges were overcome. The paper also briefly touches upon Project Management aspects, and Waterfall Vs Spiral models for development. Finally, comments are made about what key issues must be driven in order to make a project of this size and complexity achieve first silicon success.