

Tutorial on Modeling Parasitic Coupling Effects in Reliability Verification

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Abstract

As technology scaling continues in deep sub-micron domain, interconnect parasitics have become dominant in determining chip performance and functionality. R(L)C parasitics play a major role in chip performance, functionality and signal integrity. In addition, parasitics have significant impact on chip reliability due to Electromigration (EM), Timing Dependent Dielectric Breakdown (TDDB) and Channel Hot Carrier (CHC) effects. This tutorial covers several aspects of interconnect modeling from chip reliability perspective. Special emphasis is made on importance of modeling parasitic coupling in reliability analysis. A comparative study of coupled and decoupled interconnect modeling is discussed with simple examples and real life circuits.