

Tutorial Five
Electronic Testing for SOC Designers

Vishwani D. Agrawal (Coordinating Presenter)
Agere Systems, USA
va@agere.com

Michael L. Bushnell
Rutgers University, USA
bushnell@caip.rutgers.edu

Abstract

The speakers have given VLSI design and VLSI testing courses at Rutgers University for over ten years. They combine their industry and academic experiences, and believe that today's VLSI designer must know the essentials of digital, memory and mixed-signal circuits, as well as the test standards for systems that combine such components. This tutorial provides a careful selection of topics on testing of all three types of circuits and systems. The presentation is divided into three parts. Part I (Introduction) contains definition of test and its motivation, test process and automatic test equipment (ATE), test economics and product quality, and fault modeling. Part II (Test Methods) includes logic and fault simulation, testability measures, combinational and sequential ATPG, memory test, DSP-based analog test, model-based analog test, delay test, and IDDQ test. Part III (Design for Testability) covers scan design, built-in self-test (BIST), boundary scan, analog test bus, system test and testing of core-based designs. The tutorial is derived from the authors' recent textbook, *Essentials of Electronic Testing for Digital, Memory and Mixed-Signal VLSI Circuits* (Kluwer Academic Publishers, Boston, 2000, ISBN 0-7923-7991-8) and their full-semester course material available at the website <http://cm.bell-labs.com/cm/cs/who/va>.

Vishwani D. Agrawal is a Distinguished Member of Technical Staff in the Circuits and Systems Research Lab of Agere Systems (a microelectronics company to be spun off from Lucent Tech.) He holds a PhD from the University of Illinois. He is a Fellow of the IEEE. He has worked in the area of electronic testing for 30 years, has published 250 papers and 5 books and holds 13 U.S. patents.

Michael L. Bushnell is a Professor in the Department of Electrical and Computer Engineering at Rutgers University. He holds a PhD from Carnegie Mellon University. He has been a researcher in electronic testing and other VLSI related areas for over 15 years. He has published 4 books and numerous papers. He currently serves as the Graduate Director of his department at Rutgers University.