

Tutorial Four
Mathematical Methods in VLSI

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Abstract

The theme of the tutorial is the use of mathematical methods in VLSI. The traditional use of mathematics in engineering disciplines is via mathematical modeling- concepts and interactions in the problem domain are mapped to objects and relationships of a specific mathematical topic and then the formal deductions within the topic are re-interpreted in the problem domain. After a structured review of VLSI design flow and the identification of mathematical topics applicable to each step of the design flow, the tutorial illustrates these themes by a sampling of mathematical techniques applicable to analysis of modeling and simulation, partitioning, structural and behavioral decomposition, and symbolic reasoning about behavior.

The tutorial is aimed at illustrating the importance of mathematics in VLSI, especially in the development of various tools, which are critical for design. The audience will be made to appreciate how some of the tools which are used by designers actually have some very deep mathematics built into them, without which it would be impossible for any automation in the design process. This mathematics becomes more important as we go to high complexity designs involving millions of transistors, high frequencies and systems-on-chip.

The morning session will have a brief introduction on what will be covered in the tutorial, and why. This will be followed by a brief description of the existing design flow concepts, as well as how the various areas of mathematics interleave with the various aspects of design flow. There will be brief presentations and overviews of some mathematical topics which are relevant from the VLSI perspective: a) the uses of graphs and hypergraphs for modeling real life problems particularly in terms of connection, flow of information, and hierarchical construction; b) some samples of the use linear algebra in VLSI and in particular the use of eigenvalues in various contexts such as system reduction and partitioning; c) introduction to submodular functions; d) the importance of differential equations; e) classification of differential equations and some of the important ways to solve them; f) the foundations of symbolic methods used in modeling behavior for analysis and verification g) the ubiquitous 'decomposition theme'.

The afternoon session will take up a few areas of mathematics in greater detail, how they help address some the very important areas in VLSI design automation, and how they can possibly address future challenges: a) use of submodular functions for optimization problems in VLSI, their use for partitioning large scale systems which arise in many forms throughout this area is described (including the realization of large scale finite state machines through decomposition techniques and the parallel simulation of large electrical circuits); b) the use of differential equations in modeling and simulation, the SPICE equations,

their solutions using various techniques, and the relation between SPICE simulation and various other simulation scenarios; c) logical and algebraic techniques in verification d) applications of classical automaton decomposition theory.

At the end of the tutorial, we expect the audience to have a better appreciation of how mathematics is important, relevant and critical for developing design automation tools.

Dr. Madhusudan V. Atre did his 5 year integrated MSc in Physics from IIT-Bombay, with specialisation in Solid State Physics in 1978. He obtained his PhD in Theoretical Physics from IISc-Bangalore in 1985, specialising in Nonlinear Phenomena in Plasma Physics, Low Temperature Physics, and Mathematical Methods in Dynamical Systems. From 1986-1990, he was Research Associate at the TIFR-Bombay, PRL-Ahmedabad, and IISc-Bangalore, working in the areas of Mathematics of Quantum Field Theory and Dynamical Systems. In 1990 he joined the DRDO where he headed the Software Group, looking at scientific applications on parallel computers, VLSI test generation techniques, Lie-group symmetries of differential equations. He was manager of VLSI activities in Crosscheck Tech, before joining Texas Instruments in 1995 where he headed the Design Flow and Systems Engineering team, as well as the core-EDA activities. In 1998, he started the Bell Labs R&D center of the Lucent Technologies, Microelectronics Group, (now called Agere Systems after spinoff from Lucent Technologies) . As the Managing Director, he coordinates research and development in the areas of VLSI and Optoelectronics CAD, DSP software tools and applications, as well as VLSI design.

Mr. P. S. Subramanian obtained his degree in Electrical Engineering from VJTI, Mumbai in 1968. He joined TIFR, Mumbai in 1969 and worked there till 1999. He then joined Sasken Communication Technologies and is currently heading their Computer Science R&D Group working on Adaptive Embedded Systems. During his career he has worked in the areas of VLSI CAD and Computer Science ranging from the very practical to the highly theoretical. Initially, he worked in Graphics and Time Sharing Software. He then built a scientific calculator using MSIs by first designing an 8-bit processor and then microcoding CORDIC algorithms into it. He developed and made extensive use of CAD tools during this development. With this background he obtained an UNDP fellowship to study CAD in the LOCMOS facility of Philips at Nijmegen, Holland. After his return he directed a team developing a suite of CAD tools with grants from DoE. He then played an active role in a task force set up by DoE to promote VLSI activities in India. Later, he worked in areas of theoretical computer science ranging from complexity theory to semantics. He is interested in reusing the "methodologies" developed in the domain of mathematics for system design.

Prof. H. Narayanan did his B.Tech in Electrical Engineering in 1969 and his PhD in Electrical Engineering in 1974, both from I.I.T. Bombay. Since 1974 he has been with the EE Dept., I.I.T. Bombay as a faculty member and is currently a Professor. During 1983-85 he was Visiting Associate Professor at EECS, U.C. Berkeley. H. Narayanan's interest is in the area of network topology in the context of efficient network analysis. Towards this end he has worked at understanding the interactions of graph theory, matroid theory and submodular function theory with Electrical network theory. His main results in Electrical networks include a topological theory of network decomposition. In the area of matroids and submodular functions his results include the first complete description of the principal partition of a matroid (1974)(independent of N. Tomizawa of Tokyo University [1976]) and the theory of the principal lattice of partitions of a submodular function (1986). He is the author of the monograph "Submodular Functions and Electrical Networks" (Annals of Discrete Maths vol. 54). He has supervised the building of the general purpose circuit simulator BITSIM (based on topological hybrid analysis) and the point relaxation based circuit simulator BREMICS at the VLSI Design Centre, I.I.T. Bombay.