

Keynote IV

LSI Design in the 21st Century: Key Changes in Sub-1V Giga-Integration Era

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Dr Kazuo Yano is the head of the System LSI Research Department, Central Research Laboratory, at Hitachi, Tokyo. He received the BS, MS, and Ph.D. degrees from Waseda University, Japan, in 1982, 1984, and 1993, respectively. He joined the Central Research Laboratory, Hitachi Ltd. in 1984. His research interests include MOS/bipolar devices for low-temperature VLSI, CMOS/BiCMOS logic circuits, single-electron devices, System-level LSI design methodology, and CAD tools. From 1991 to 1992, he was a Visiting Scientist at the Arizona State University, working on single-electron transport physics with Prof. D. K. Ferry. He has conceived the complementary pass-transistor logic (CPL), and has done pioneering work on the synthesis of pass-transistor logic circuits (LEAP) and nano-structured (single-electron) memories. He is supervising research teams on Hitachi's microprocessors, microcontrollers and system-on-a-chip-related research. He is a co-author of the book *Silicon-Based Hetero-junction Devices* (Maruzen, 1991) and *The VLSI Handbook* (CRC Press and IEEE Press, 2000). He is a member of the IEEE, the Japan Society of Applied Physics, and the IEICE of Japan. He received the IEEE Paul Rappaport Award in 1994, the IEEE Lewis Winner Award in 1996, and the IEEE Jack Raper Award in 1998. He has been a member of the solid-state device sub-committee of IEDM.

Abstract

The conventional CMOS technology will face difficulty in sub-0.1 μm , sub-1V region, where it will inevitably deviate from conventional straightforward roadmap. Random-modulation CMOS, which assigns multiple threshold levels in the same block through the use of sophisticated CAD tools, will emerge as a key technology in this new regime. Beginning with this first step, the era of “complex CMOS,” which requires complicated design elaborations and operating control, is predicted to begin. This key change will open up opportunities for new methodologies and CAD tools. Another major change in trend will be the shift in System-on-Chip design methodology from being processor-centric to either memory-centric or communication-centric, depending on the application. In the former case, nano-structured memory technology will be a key innovation, which requires completely new design expertise, including quantum physics, and tools. In the latter case, real IP reuse is the key, which will be enabled by a new specification language, such as the *Object Wrapper language*. Our efforts to standardize this new language and its design methodology will also be introduced.