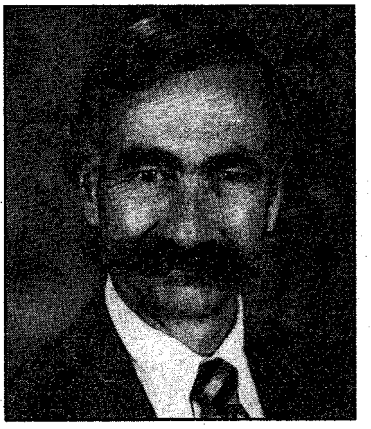
Design for Testability: Today and in the Future



T.W. Williams
IBM Technology Products
Boulder, Colorado, USA

With continued increases in densities of technologies, testing continues to be a significant impediment to productivity if not addressed properly. In this presentation we will review the current techniques with a particular emphasis on today's Scan Designs. This will entail distinguishing the differences between scan techniques, since all scans are not created equal! From this point the Testability Standards will be discussed; this will include the Boundary Scan activities and the Analog activities. Fault models are taking on more robust attributes, since the Stuck-At-Fault is necessary but not sufficient in today's technologies. The Delay Fault models will be discussed with a comparison between a model which increases exponentially with gate count (Path Delay Fault) and one which increases linearly with gate count (Gate Delay Fault). Clearly, self-test is taking on an ever more important role which impacts both manufacturing testing and field system testing. The popular self-testing design techniques will be shown. This presentation will discuss the interaction of testing and synthesis with a view on delay. Finally, the role of testing will be explored in the new design environments which includes Hardware and Software Codesign.

Biography

Thomas W. Williams

Thomas W. Williams is a Senior Technical Staff Member with IBM Microelectronics Division in Boulder, Colorado. He is currently the manager of the VLSI Design for Testability group, which deals with design for testability of IBM products. He received a BSEE from Clarkson University, and MA in pure mathematics from State University of New York at Binghamton, and a PhD in electrical engineering from Colorado State University. Dr. Williams is engaged in numerous professional activities. He is the founder and chair of the annual IEEE

Computer Society Workshop on Design for Testability. He is the co-founder of the European Workshop on Design for Testability. He is also the chair of the IEEE Technical Subcommittee on Design for Testability. He has been a program committee member of many conferences in the area of testing, as well as being a keynote or invited speaker at a number of conferences, both in the U.S. and abroad. He was selected as a Distinguished Visiting Speaker by the IEEE Computer Society from 1982 to 1985. He has been a special-issue editor in the area of design for testability for both the IEEE Transactions on Computers and the IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems. He has written four book chapters and many papers on testing, edited a book and recently co-authored another book entitled *Structured Logic Testing* (with E. B. Eichelberger, E. Lindbloom, and J. A. Waicukauski). Dr. Williams has received a number of best paper awards, including the 1987 Outstanding Paper Award from the IEEE International Test Conference for his work in the area of VLSI Self-Testing (with W. Daehn, M. Gruetzner, and C.W. Starke), a 1987 Outstanding Paper Award from the CompEuro '87 for his work on Self-Test, a 1989 Outstanding Paper Award (Honorable Mention) from the IEEE International Test Conference for his work on AC Test Quality (with E.S. Park and M.R. Mercer), and a 1991 Outstanding Paper Award from the ACM/IEEE Design Automation Conference for his work in the area of Synthesis and Testing (with B. Underwood and M. R. Mercer). He is an Adjunct Professor at the University of Colorado, Boulder, and in 1985 was a guest professor and Robert Bosch Fellow at the University of Hannover in Hannover, Germany. Dr. Williams was named an IEEE fellow in 1988 for leadership and contributions to the area of design for testability. In 1989, Dr. Williams and Dr. E. B. Eichelberger shared the IEEE Computer Society W. Wallace McDowell award for Outstanding Contribution to the Computer Art, and was cited for developing the level-sensitive scan technique of testing solid-state logic circuits and for leading, defining, and promoting design for testability concepts. His research interests are in design for testability (scan design and self-test), test generation, fault simulation, and synthesis.