

TUTORIAL 3: PHYSICAL DESIGN

Presenters:

D. Mehta, University of Tennessee Space Institute, USA

N. Sherwani, Intel Corp., CA, USA (sherwani@ichips.intel.com)

Coordinator:

A. Bariya, Intel Asia Electronics, Ltd., Bangalore, India

Description: The objective of the tutorial is to survey recent algorithms and methodologies that have had (or are likely to have) a significant impact on the physical design industry. A second objective is to provide industrial feedback to the academic community in an effort to increase the relevance of academic research to industrial needs. Outline: Data Structures for VLSI, Partitioning, Floorplanning, Placement, Routing, Post-routing Optimizations, Physical Design of FPGAs, Physical Design of MCMs.

D. Mehta (Ph.D. Univ. of Florida), Assistant Professor at the University of Tennessee Space Institute, co-author of Fundamentals of Data Structures in C++ with E. Horowitz and S. Sahni, has research interests in algorithms for VLSI physical design automation and parallel computing.

N. Sherwani (Ph.D. Univ. of Nebraska-Lincoln), is with Intel Corporation and currently leads the project on Full Chip layout. His work at Intel concentrates on physical design tools and methodologies for layout of microprocessors with very high frequency goals.

TUTORIAL 4: VERIFICATION

Presenters:

R. Raina, Motorola Inc., Austin, TX, USA (raina@ibmoto.com)

J. Abraham, Univ. of Texas, Austin, TX, USA (jaa@cerc.utexas.edu)

Coordinator:

A.K. Pujari, Central University, Hyderabad, India

Description: This tutorial will cover all aspects of the newly emerged area of VLSI Design Verification, including Microprocessor Verification, Multi-Media Design Verification and the use of Formal Methods. The tutorial will describe the profile of a newly emerged group of VLSI designers — the Design Verification Engineers. Existing state-of-the-art tools from various universities, will be described and demonstrated, running on a laptop under Linux.

R. Raina (Ph.D. Duke Univ.), is a staff engineer with Motorola, working on Power PC microprocessor design. His interests include verification, logic design, and design-for-testability.

J. Abraham (Ph.D. Stanford Univ.), is a professor in the ECE Department at the University of Texas, Austin. His research interests include VLSI design and test, formal verification, and fault-tolerant computing.