

Tutorial 4: VLSI IMPLEMENTATION OF DSP ARCHITECTURES

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We present programmable vendor DSP architectures. We discuss technology, architectural, and performance trends of first, second, and third generation embedded DSP processors. We cover synthesis of high performance algorithm-specific architectures for real-time signal processing using function-preserving transformations that convert an algorithm signal flow graph into a high-performance microarchitecture. Case studies highlight area/power minimization tradeoffs.

Arupratan Gupta (MS Washington State '83) manages wireless and multimedia efforts at AT&T Bell Labs. His interests are voice messaging and DSP architectures.

V. Visvanathan (PhD U. of Calif., Berkeley) is an Assoc. Prof. at IISc, Bangalore. He has the Distinguished Tech. Staff Award at AT&T Bell Labs('88) and an Hon. Mention Award at VLSI Design '93.

Tutorial 5: HARDWARE SOFTWARE CO-DESIGN OF EMBEDDED SYSTEMS

R. Gupta - Computer Science Dept., U. of Illinois, Urbana, IL (rgupta@cs.uiuc.edu)

We cover CAD and synthesis of digital embedded systems, more specifically systems consisting of interacting hardware and software components. We will initially review fundamental concepts in embedded system modeling and analysis. Secondly, we present recent advances in compilation techniques for both hardware and software. We describe issues in interface modeling and optimization. Finally, we describe simulation for embedded system design.

Rajesh Gupta (PhD Stanford '94) is currently an Asst. Prof. of Computer Science at the Univ. of Illinois. Previously, he was a Senior Design Engineer at Intel ('87-'89). His interests are VLSI design automation algorithms, CAD for embedded and real-time systems, and VLSI design at various levels of abstractions.

Tutorial 6: PRACTICAL TEST AND DFT FOR NEXT GENERATION ULSI

J. Abraham - ECE Dept., Univ of Texas, Austin, TX (jaa@cerc.utexas.edu)

G. Ganapathy - Advanced Micro Devices, Austin, TX.

This tutorial is for designers and test engineers who test huge multi-million transistor chips. We discuss chip testing approaches for both logic and delay-related defects, and point out their limitations for complex designs. We discuss practical design for testability and test generation techniques for such designs that do not worsen area and performance. Examples will be multi-million transistor industrial processors, including the AMD K5 superscalar processor.

Jacob Abraham (IEEE Fellow, PhD Stanford '74) is a chaired Prof. at the U. of Texas. He works on test and design for testability. He has 200 papers and directed over 30 PhD's.

Gopi Ganapathy worked on test generation and fault simulation for full-custom, million transistor microprocessors at AMD. He has 7 testing patents and a Best Paper Award at the Design Auto. Conf. ('93).