

# Tutorials - VLSI Design '96

Wednesday, January 3, 1996

PARALLEL TUTORIAL SESSIONS

9:00 AM-5:00 PM

## Tutorial 1: LOW POWER DESIGN

**K. Roy** - Purdue University, USA (kaushik@ecn.purdue.edu)

**R. K. Roy** - NEC C&C Research Laboratory, USA (roy@cctl.nj.nec.com)

This tutorial is for system and ASIC designers, CAD developers, managers, and researchers. The low power design areas covered include: (1) The importance of low power design, (2) Power estimation, (3) Logic and circuit design, (4) System design, (5) Power issues for memories, disks, and displays, (6) Software issues, (7) The power dissipation impact on system reliability, (8) CAD tools, (9) An example design, and (10) Future trends.

**Kaushik Roy** (PhD U. of Illinois, Urbana '90) is an Asst. Prof. at Purdue ('93). He received the 1995 NSF Career Development Award. His interests are low-power design, testing, fault tolerance, and FPGA's.

**Rabindra K. Roy** (PhD U. of Illinois, Urbana) has interests in testing, synthesis for testability, and low power design. He has two Best Paper Awards at VLSI Design '94.

## Tutorial 2: REGISTER TRANSFER LEVEL SYNTHESIS: FROM THEORY TO PRACTICE

**K. Keutzer** - Synopsys Inc, USA (keutzer@synopsys.com)

**S. Malik** - Princeton University, USA (sharad@ee.princeton.edu)

This tutorial will cover all aspects of the synthesis of digital systems from RTL (Register Transfer Level) descriptions to optimized gate-level netlists. Emphasis will be placed on fundamental techniques that have worked successfully in practice. These will include technology independent, as well as technology specific, optimizations. The only prerequisite for the tutorial is a basic knowledge of logic design.

**Kurt Keutzer** (PhD Indiana U. '84) is Chief Scientist at Synopsys Inc., and leads researchers in design synthesis/verification. He is on the editorial boards of two journals.

**Sharad Malik** (PhD University of Calif., Berkeley '90) is an Asst. Prof. at Princeton University. He was awarded the President of India's Gold Medal ('85), the IBM Faculty Development Award ('91), and the NSF Young Investigation Award ('94).

## Tutorial 3: MIXED-SIGNAL DESIGN FOR TEST

**Bapiraju Vinnakota** - University of Minnesota, USA (bapi@ee.umn.edu)

**Ramesh Harjani** - University of Minnesota, USA (harjani@ee.umn.edu)

The increasing availability of complex analog and mixed-signal ICs makes systematic test techniques important. This tutorial will discuss the merits and costs of recent design-for-testability techniques for analog and mixed-signal circuits. The classification of DFT techniques will be based on the analog/mixed-signal circuit functionality. The discussion is oriented towards designers and covers circuits most commonly used in practice.

**Bapiraju Vinnakota** (BTech IIT Madras '87, PhD Princeton '91) is an Asst. Prof. at Minnesota. He has a National Science Foundation (NSF) Career award ('95).

**Ramesh Harjani** (BTech BITS, Pilani '82, MTech in EE IIT, Delhi '84, PhD Carnegie Mellon '89) is an Asst. Prof. at Minnesota ('90). He received the NSF Research Initiation Award ('91).