

# Technique to Design MLP's Networks in CMOS Technology with Adjustment of the Back-Propagation Algorithm

Fabio de Albuquerque Pereira and J es Jesus Fiais Cerqueira

Departamento de Engenharia El trica da UFBA

Rua Aristides Novis, 02, Federa  o, Salvador-BA, CEP:40210-630, Brazil

E-mail: {fabioap, jes}@ufba.br

Conception of structures in CMOS technology that demand low power and low silicon area consumption have been widely investigated in the implementation of artificial neural networks in VLSI integrated circuits for signal processing purposes [2], [6]. *Feedforward* MLP networks' building blocks require CMOS multipliers for implementing the synapses and the activation function circuits. A larger scale of integration of such networks happens at the expense of simpler and, as a result, nonlinear synaptical blocks. Regarding these aspects it becomes advisable to derive suitable expressions to adjust the back-propagation algorithm and deal with these nonlinearities [5].

The implementation of CMOS multipliers have been based on the use of either analog circuits for continuous time signal processing or switched current techniques for discrete time processing, once current mode topologies have become a trend for IC designers in low voltage applications. In this work we perform an analysis of some techniques for implementing the basic building blocks in a neural network in IC technology for analog signal processing. Even though we focus on the operation of MOS devices in the strong inversion region deep into saturation, some aspects of the synapses in the weak inversion region [3] are also explained, which has been accomplished through the use of classical asymptotical models for the drain current [4].

Through the proper adjustment of the back-propagation algorithm one might overcome the intrinsic nonlinearities of CMOS synaptic multipliers and avoid that the training of the network eventually fails to converge at some point in time. It's also presented that the learning rate (that controls the convergence of the method) will depend on the bias conditions and on the transconductance parameter that includes itself technological parameters, geometry and device's dimensions as well. In order to maintain the algorithm convergence it's required that this learning rate does not exceed an well defined upper bound [1].

The choice of the learning rate is a crucial decision for convergence of the algorithm. If the learning rate is too low,

the convergence will be very slow due to the large number of iterations needed and the velocity of the neural network will be rather unsatisfactory. If the learning rate is high, in the beginning the convergence will be very fast, but the it might diverge in the later cycles of training. Towards that end it's important for IC designers to take into account these features and search for a trade-off solution between the number of neuronal structures per chip and an optimized performance of the neural network regarding its learning time.

## References

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