

Keynote Address

Polymorphic Processors: How to Expose Arbitrary Hardware Functionality to Programmers

Stamatis Vassiliadis
T. U. Delft, The Netherlands

Summary: In this talk we present a polymorphic processor paradigm incorporating both general purpose and custom computing processing. This family of processors incorporates an arbitrary number of programmable units, exposes the hardware to the programmers/designers, and allows them to modify and extend processor functionality at will. To achieve the previously stated attributes, we discuss a new programming paradigm, a new instruction set architecture, a microcode-based microarchitecture, and a compiler methodology. The programming paradigm, in contrast with the conventional programming paradigms, allows general-purpose conventional code and hardware descriptions to coexist in a program. In the polymorphic processor paradigm, it is shown that for a given instruction set architecture an one-time instruction set extension is sufficient to implement the reconfigurable functionality of the processor. We also discuss some microarchitectural issues and suggest that hardware emulation could allow high-speed reconfiguration and execution. We also discuss several design issues for polymorphic compilers. We also provide some evidence suggesting that the polymorphic paradigm could provide performance gains when compared to stand-alone hardwired microprocessors. We also present experiments for the MPEG-2 encoder and decoder with a polymorphic processor prototype implemented in the Xilinx Virtex II Pro FPGA. We show that the overall attainable application speedup for the MPEG-2 encoder and decoder is between 2.64 and 3.18 and between 1.56 and 1.94, respectively, representing between 93% and 98% of the theoretically obtainable speedups.