

SEED2002

Support of Educational course for Electronic Design

Patrick R. Schulz*, Ulrich Brüning*, Gunter Strube[#]

*Computer Architecture Group
University of Mannheim
68131 Mannheim, Germany
schulz@uni-mannheim.de

[#] VCAD Services
Cadence Design Systems GmbH
85622 Feldkirchen, Germany
gunters@cadence.com

ABSTRACT

This paper summarizes the content and application of the SEED2002 project. SEED2002 is a university/industry collaboration to enhance and reform the education in the field of semi-custom/full-custom ASIC design at the universities of Mannheim, Heidelberg and Kaiserslautern, Germany. With this project Cadence Design Systems enables us to teach leading-edge ASIC design using their most innovative products.

1. Introduction

It's not a secret that for efficient use of most EDA tools an amount of experience is needed, that students typically don't have. Teaching these tools practical courses or exercises including the challenges imposed by the latest technological advances requires a thorough understanding of the underlying methodologies and up to date practices. Students have to deal with a lot of new skills at the same time and the complexity of the things to be considered can easily lead to frustration. Therefore, most universities try to avoid practical work in the field of backend (physical) design, work with simplified methodology and older technology, or even leave the ASIC domain to favor FPGAs.

Together with Cadence Design Systems and SEED2002 we took a step forward. Beginning with this semester (mid of october to mid of february) we teach a lecture and practical course named 'Semi-Custom Design Flow' (SCDF), where our students learn the methodology of high-speed nanometer ASIC design by the use of the most innovative EDA tools. These include Physically Knowledgeable Synthesis (PKS), FirstEncounter, Nanoroute, CeltIC and Fire&Ice supported by Cadence Design Systems. This lecture and practical course affiliates perfectly to the lecture 'hardware design', that has been held for years now and covers (architectural) system, interface and digital circuit design using Verilog HDL.

2. University/Industry Cooperation

This university/industry cooperation represents a win-win situation for both partners, Cadence Design System and the later pictured ASIC Competence Center consisting of the universities of Mannheim, Heidelberg and Kaiserslautern. By means of this project we want to achieve a long-term relationship between Cadence Design Systems and the ASIC Competence Center.

We understand the importance of the design environment for our business and recognize Cadence's experience in electronic design,

electronic design automation and design environments. We wish to improve the quality and efficiency of our design process by utilizing Cadence tools.

Cadence will use its experience in design environments to help us by creating and maintaining design environments focused on our requirements. This will help us to reduce internal efforts and allow us to focus our efforts on education and research. By virtually integrating Cadence engineers into our Computer Aided Design ("CAD") activities, we will benefit not only from the experience of the specific engineers, but also from a direct channel to Cadence's know-how network. This will typically result in a more reliable design environment designed for flexibility and also in a faster and smoother integration of technology enhancements. For us, this will provide the possibility of designing higher quality designs, within shorter design cycles.

Additionally we got access to Cadence's Sourcelink, a to Cadence users restricted documentation database that contains application/technical notes, known problems and workarounds, as well as customer focused solutions from Cadence VCAD services. These so called 'VCAD-IPs' are for example tools like the 'Design Environment Configuration Manager' (DECM) or the 'Semi Custom WorkBench' (SCWB) as well as design flows and interfaces to third-party vendors.

3. Education

Like the afore mentioned lecture and practical course 'Semi-Custom Design Flow' all participating universities are going to found new lectures and courses or restructure existing ones in the way that the whole design flow is covered. The main focus during this work is to develop practical exercises suitable for student work but also complex enough to face the problems of real-world designs. Missing tool experience is compensated by experts from Cadence VCAD Services in Feldkirchen, Germany.

The expertise of the participating groups define the advanced subject course curriculum. It ranges from the afore mentioned:

- high-level system and interface design,
- synthesis, place and route, extraction, static timing analysis (the whole cell-based design flow),
- to full custom analog and standard cell design and
- the integration of both worlds by timing, power and functional characterization and abstract generation.

4. Participants

The **ASIC Competence Center (ASICCC)** is a fusion of three research groups from the University of Mannheim, the University of Heidelberg and the University of Kaiserslautern, with the intention to bundle resources in the area of teaching *Hardware and Chip-Design* and to share the expert knowledge among the groups. An advanced design flow for semi-custom chip design in an actual technology (UMC 0.18 μ m) is supported by the center. The following three groups are currently members of the ASICCC.

The **Computer Architecture Group** [2] at the University of Mannheim holds a profound expert knowledge in the area of hardware-, computer architecture- and interconnection network design, especially for the construction of large computing clusters based on PC technology [5]. In the area of education the group is responsible for the advanced course on *Hardware and VLSI design*, which covers the complete design process from specification, design space exploration, RTL coding and simulation to the back end flow of a target technology.

The **Computer Engineering Group** [3], Kirchhoff-Institut für Physik, at the University of Heidelberg is specialized on applications and improvements of computer systems in physics. Design solutions are used at current experiments at CERN. One example is the first level trigger, that is capable of tracing 16000 particles in a 15 Terabyte/sec dataflow using 65000 MIMD processors [6]. This group has a complete ASIC laboratory including cleanrooms, bonders, and wafer probers.

The **Microelectronic Group** [4], at the University of Kaiserslautern is developing analog full custom designs. The research focus of this group ranges from high performance custom I/O cells, that are compatible to the semi custom flow, over high resolution analog digital converters (ADCs) and laser drivers to phased locked loops (PLLs).

Cadence VCAD [1] is a unique service to provide design system life-cycle support service to build an integrated EDA infrastructure, implementing and managing customers design environment from early-stage design system architecture and planning, design system and flow implementation, and ongoing operations and enhancement support. By leveraging a collaboration infrastructure a broad range of expertise can be made available providing comprehensive and rapid issue resolution throughout all design phases.

The VCAD approach allows Customers to focus on its primary objective of architectural and product design, relying on VCAD's core competency to manage its design infrastructure and help them implement and verify the design. The fast, flexible and comprehensive VCAD support minimizes risk and becomes a vital enabler for the first time right completion of designs.

5. First results

At the end of this semester (mid of February) the first students will have their graduate exams in 'SemiCustom Design Flow'. In the lecture we started with the traditional design flow described in T. Abbasi's book "It's the methodology, stupid!", covered IEEE 1364.1 Verilog RTL Synthesis, standard tool interfaces, IP cores and finally focused on new EDA methodologies especially in the nanometer area. In the practical course emphasis was placed on tool usage with real-world designs. For this course we used an Ethernet MAC core donated by Get2Chip (thanks to Taher Abbasi) in a 0.18 μ m UMC logic process and standard cells from Virtual Silicon Technology. The students were given the synthesized

netlist of the MAC core and asked to 'make a chip'. They started with a simple Floorplan, placed macros, added power/ground rings, placed the standard cells, did the clock tree synthesis and so on down to the constrained timing violation free physical design. They learned the influence of the sequence and the importance of constraints of the various design flow steps. Another task they had to cope with was plain logic synthesis of a XBAR design, which is a subblock of a research project called ATOLL[5]. The students from this first course are showing high interest to continue in the direction of digital ASIC design and apply the learned skills in industrial environments. Two students are planning to do an internship at Cadence's VCAD Services, one is going to do his master thesis at the ASIC Design group of IBM in Böblingen, Germany. Other graduate students and graduates that passed our curriculum were rated by the Group Leader of 'Automotive Driver Information ASSP Design' at Toshiba Electronics Europe GmbH. He said: "It is ideal for us, if students get an overview of the entire VLSI process chain (from front-end down to testing prototypes). This is outstanding for Mannheim's graduates, I didn't have the opportunity at my university".

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