

# Performance Analysis of A Banyan Based ATM Switching Fabric with Packet Priority

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## Abstract

*In this paper, we propose a new model for the performance analysis of an ATM switching fabric based on single-buffered Banyan network. In this model, we use a three-state, i.e., "empty", "new" and "blocked" Markov chain model to describe the behavior of the buffer within a switching element. In addition to traditional statistical analysis including throughput and delay, we also examine the delay variation. Performance results show that the proposed model is more accurate in describing the switch behavior under uniform traffic environment in comparison with the "two-state" Markov chain model developed by Jenq [4] and Yoon [6]. Based on the "three-state" model, we study a packet priority scheme which gives the blocked packet higher priority to be routed forward during contention. For a fully loaded six-stage switch, the analytical model predicts that the delay variation can be reduced by 35%, while the simulation shows a 22% reduction.*

## I. Introduction

The Broad-band Integrated Services Digital Network (B-ISDN) is a computer communication network which provides multimedia services including voice, video and data traffic with high bandwidth capacity and flexible switching technology. The Asynchronous Transfer Mode (ATM) has been recommended by CCITT (now ITU) and ATM Forum as the transport technology to support future B-ISDN. ATM is a cell based fast packet switching technology in which information from different sources are packetized into small packets called ATM cells with the same length (53 bytes) and transmitted over a single broad-band network. As the essential part of ATM networking, the switching architecture and its performance have been studied extensively by many researchers in the data communication area.

Among the many candidates of the ATM switching fabrics, Banyan networks have been proposed in several publications [1] - [13] for the implementation of an ATM switching node. The Banyan network is a multistage interconnection network that was originally proposed for supporting communication between processors and memory modules in large scale multiprocessor system. Because of its self-routing characteristic and simplicity in hardware, it has also been used as a fast packet switching fabrics in communication networks.

Since the switch plays a critical role in the overall performance of the computer network, the performance analysis of the switching fabric is important for researchers and designers of ATM network. The performance analysis of the Banyan network has been under extensive study in past few years. Patel [2] analyzed the performance of unbuffered Banyan network under uniform traffic pattern and provided a recursive algorithm for the throughput of the switching network. Kruskal and Snir [5] further provided the asymptotic solution for this recursive algorithm for the Banyan network with infinite buffer size. Jenq [4] as well as Dias and Jump [3] extended Patel's work by analyzing the performance of single-buffered Banyan network under uniform traffic. In Jenq's paper [4], a simple analytic model is provided in recursive form to analyze the throughput and delay of the single-buffered Banyan network that consists of  $2 \times 2$  crossbar switching elements (SE). Yoon, et, al.[6] extended Jenq's model by analyzing the performance of multibuffered Banyan network consists of SEs with arbitrary size. On the other hand, Wu [8] and Kim [9] studied the performance of buffered Banyan network under nonuniform traffic patterns. The performance of buffered Banyan networks placed in parallel was also studied by Kim [9] [11].

Since the Banyan network is a blocking network, contention occurs when two packets from different buffers within the same SE are destinating the same output port of that SE. In this case, one packet has to be blocked for

one clock cycle. In the previous studies, it is assumed that the blocked packet will generate a new random destination during the next clock cycle. This assumption causes inaccuracy in the performance evaluation of the Banyan switch. As was pointed out by Yoon [6], the analytic results based on this assumption are more optimistic than simulation results. In order to more accurately describe the behavior of the switching element in a single-buffered Banyan network, we introduce a simple "three-state" Markov chain model to distinguish a packet that has not been blocked before in a buffer and a packet that has been blocked for at least one time in that buffer. This model should improve the accuracy of previous models by Jenq [4] and Yoon [6]. In this new model, it is assumed that the blocked packet will still be destinating the same output port in the next clock cycle. Similar models [7] [14] are also proposed to improve the inaccuracies in Jenq's model [4] by introducing another state to indicate whether a packet in a buffer has been blocked previously. However, the analytic model in [7] was derived by exhaustively tracing the possible states of input buffers in each SE, the generalization of this model to the case of multiple buffers and arbitrary size SEs is difficult. A modified model independent of the sizes of SEs was introduced by Hsiao and Chen [14]. That model shows slightly more accuracy, but it is still complicated in the analysis of the state transitions. Also only the throughput and delay were studied in [14]. For ATM switches, the variation of the delay is an important parameter for delay sensitive services like audio and video. In this paper, we use the moment generating function to analyze the variance of the network delay for the proposed "three-state" model. We also introduce a packet priority scheme by giving the "blocked" packet higher priority of being able to move forward when it is contending the same output port with a packet that has never been blocked before. By doing this, one can expect to reduce the variance of the network delay. Although the model developed in this paper is based on single buffer banyan network, it can also be extended to multiple buffer banyan network.

In Section II, the structure and operation of single-buffered Banyan network are described. In Section III, the proposed "three-state" Markov chain model is introduced. This is followed by a complete mathematical model in Section IV that describes the relations among the steady-state probabilities in the "three-state" model. Comparisons of performance results with previous model are also made in this section. In Section V, a new routing logic with packet priority is introduced to reduce the variance of the network delay and modifications on the analytical model as well as performance results are obtained. Finally, the paper concludes in Section VI.

## II. Structure and Operation of the Single-Buffered Banyan Switch

The single-buffered Banyan network is a multistage interconnection network with stages consisting of an array of switching elements. Each switching element is a  $2 \times 2$  crossbar switch with a single buffer at each of its input links. The switching element is linked to its adjacent stages in a particular interconnection pattern such that a unique path can be established from any one of the input ports of the network to any one of its output ports. The structure of a  $16 \times 16$  single-buffered Banyan network is shown in Fig. 1. For a Banyan network with  $N$  input ports and  $N$  output ports, the number of stages in the switching network is  $\log_2 N$ . A more detailed description of the interconnection patterns among the switching elements of the Banyan network is given by Patel [2].

The Banyan network based ATM switch operates synchronously. In the first part of the clock cycle, control signals are passed across the network from the last stage toward the first stage, so that every port of the network can determine whether to send or hold its packets. Then in the second part of the clock cycle, packets move in accordance with the control signals.

The switching element in the first stage sends the packet according to the first bit of the destination address. "0" or "1" will route the packet to the upper output port and to the lower output port, respectively. The  $n$ th stage switching element will perform the same function according to the  $n$ th bit of the destination address.

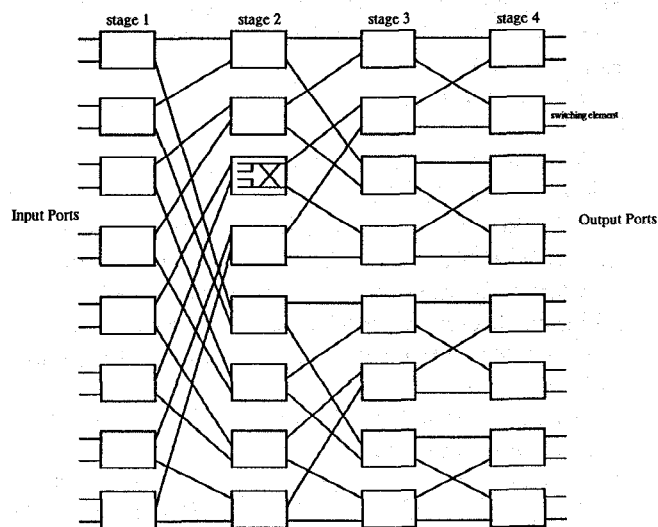


Fig. 1 Structure of A  $16 \times 16$  Buffered Banyan Network

A packet is allowed to advance to the next stage if the buffer in the next stage is empty or if the buffer is about to become available because its packet can advance at the same clock cycle. A conflict arises when there are packets in both the upper and lower buffers that are destined to the same output port. In this case, a "blocked" packet has the higher priority of moving forward if it is competing with a "new" packet. Otherwise, one packet is chosen randomly to advance to the next stage, and the other one remains in the buffer. This scheme of packet priority during contention is expected to reduce the variance of the network delay.

### III. Markov Chain Model of Switching Element with Single Buffer ( 2 x 2 cross-bar SE )

In this section, we describe the Markov chain model for the single buffer in a switching element of the Banyan network under uniform traffic. The model proposed here is based on the two-state Markov chain model developed by Jenq [4]. In the previous "two-state" model, it is assumed that the blocked packet will generate a new random destination during the next clock cycle. This is not a realistic assumption because the packet that has been blocked in the previous clock cycle will assume the same output port in the next clock cycle. In order to distinguish between the state in which the buffer contains a packet that has just arrived in the previous clock cycle and the state in which the buffer contains a packet that at least once, we introduce a third state for the case that the buffer contains a blocked packet to modify the previous model. The following is a brief description of the states of the new model:

"e": the state that the buffer in a switching element is empty;

"n": the state that the buffer in a switching element contains a "new" packet;

"b": the state that the buffer in a switching element contains a "blocked" packet.

A "new" packet is a packet in the buffer that has just arrived in the previous clock cycle. A "blocked" packet is a packet in the buffer that has been blocked for at least once.

We first define the following probabilities to be used in the analytical model:

1.  $P_{i,j}^k$  : the steady state probability that there is  $i$  packet of type  $j$  in the buffer of an SE at stage  $k$ , where  $i = 0, 1$  and  $j = "e", "n", "b"$ , corresponding to the

three states of the buffer in the Markov chain model. Notice that when  $i = 0$ ,  $j$  can only be "e".

2.  $q^k$  : the probability that a packet is ready to come to a buffer of an SE at stage  $k$ .

3.  $r_n^k$  : the probability that a "new" packet is able to move forward to the next stage given that there is a "new" packet in the buffer of an SE at stage  $k$ .

4.  $r_b^k$  : the probability that a "blocked" packet is able to move forward to the next stage given that there is a "blocked" packet in the buffer of an SE at stage  $k$ .

We use Markov chain to describe the transition of the three states of a single buffer. As shown in Fig. 2. The state of a buffer changes from "e" to "n" when there is a packet ready to come to this buffer. The state of a buffer remains at "e" when there is no packet ready to come to this buffer. When the state of the buffer is in "n", it changes to state "e" when there is no packet ready to come to the buffer and the packet in the buffer is able to move forward to the next stage. When there is a packet ready to come to the buffer and the packet in the buffer is able to move forward to the next stage, the buffer remains in state "n". When the packet in the buffer is not able to move forward, the state of the buffer changes from "n" to "b". When the state of the buffer is in "b", it changes to state "e" when there is no packet ready to come to the buffer and the packet in the buffer is able to move forward to the next stage. When the packet in the buffer is not able to move forward, it remains in state "b". The state of the buffer changes from "b" to "n" when there is a packet able to come to the buffer and the packet in the buffer is ready to move forward to the next stage.

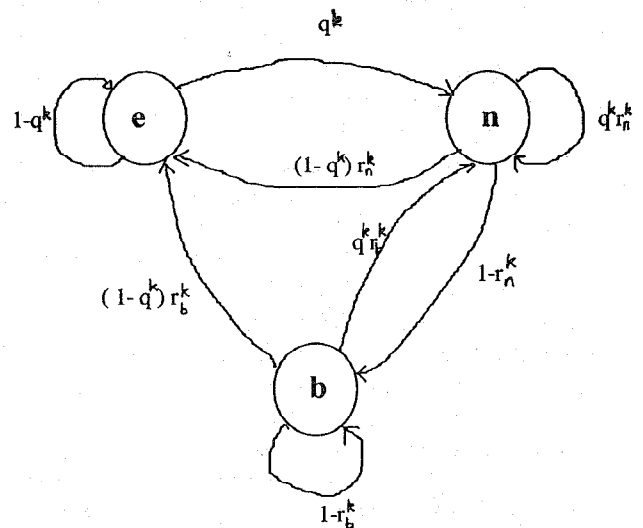


Fig. 2 The State Transition Diagram of A Single Buffer

#### IV. Performance Analysis of the Banyan Switching Fabric Without Packet Priority

In this section, we first present the state transition equation that governs the behavior of the single buffer of a switching element in the Banyan switch fabric. We then derive the relations among the steady state probabilities and obtain an recursive algorithm for calculating the performance parameters of the switch. Finally, we show the performance results based on the proposed "three-state" model and compare them with those of the previous "two-state" model. In this paper, we only study the performance of the switching fabric. Therefore, it is assumed that there is an infinite size buffer at each input port of the switching fabric for the storage of those packets that cannot enter the switch.

##### The Analytic Model

The state transition equations of the Markov chain model of the Banyan switching fabric described in Section II are stated as follows:

$$\begin{pmatrix} p_{0,e}^k(t+1) \\ p_{1,n}^k(t+1) \\ p_{1,b}^k(t+1) \end{pmatrix} = T \cdot \begin{pmatrix} p_{0,e}^k(t) \\ p_{1,n}^k(t) \\ p_{1,b}^k(t) \end{pmatrix} \quad (1)$$

where  $T$  is the state transition matrix and

$$T = \begin{pmatrix} 1-q^k & (1-q^k)r_n^k & (1-q^k)r_b^k \\ q^k & q^k r_n^k & q^k r_b^k \\ 0 & 1-r_n^k & 1-r_b^k \end{pmatrix} \quad (2)$$

Let us now derive the recursion for evaluating  $r_n^k$ .

A "new" packet is able to move forward if it is ready to move forward and the destined buffer at the next stage can accept a packet. A "new" packet at stage  $k$  is ready to move forward when one of the following events occurs:

- 1) There is no packet in the neighbouring buffer of that SE;
- 2) There is a "new" packet in the neighbouring buffer of the SE, but the considered packet wins the contention;
- 3) There is a "blocked" packet in the neighbouring buffer of the SE, but the considered packet wins the contention;

Therefore, the probability that a "new" packet at stage  $k$  is ready to move forward is

$$p_{0,e}^k + 0.75 p_{1,n}^k + 0.75 p_{1,b}^k$$

The probability that a buffer at stage  $k$  can accept a packet is

$$p_{0,e}^k + p_{1,n}^k r_n^k + p_{1,b}^k r_b^k$$

Therefore, we have

$$r_n^k = (p_{0,e}^k + 0.75 p_{1,n}^k + 0.75 p_{1,b}^k) \cdot (p_{0,e}^{k+1} + p_{1,n}^{k+1} r_n^{k+1} + p_{1,b}^{k+1} r_b^{k+1}) \quad (k = 1, 2, 3, \dots, n-1) \quad (3)$$

and for  $k = n$ , we have

$$r_n^n = p_{0,e}^n + 0.75 p_{1,n}^n + 0.75 p_{1,b}^n$$

at the last stage of the switch.

The derivation of  $r_b^k$  is similar to that of  $r_n^k$  except the following observation:

Since the considered packet has been blocked and it will go to the same input buffer at the next stage (stage  $k+1$ ). Thus we know that the destined buffer at stage  $k+1$  can only be in either state "n" or state "b" at the beginning of the current clock cycle. Therefore, the probability that the buffer at stage  $k+1$  can accept a packet is

$$\frac{p_{1,n}^{k+1}}{p_{1,n}^{k+1} + p_{1,b}^{k+1}} \cdot r_n^{k+1} + \frac{p_{1,b}^{k+1}}{p_{1,n}^{k+1} + p_{1,b}^{k+1}} \cdot r_b^{k+1}$$

Hence we have,

$$r_b^k = (p_{0,e}^k + 0.75 p_{1,n}^k + 0.75 p_{1,b}^k) \left( \frac{p_{1,n}^{k+1}}{p_{1,n}^{k+1} + p_{1,b}^{k+1}} r_n^{k+1} + \frac{p_{1,b}^{k+1}}{p_{1,n}^{k+1} + p_{1,b}^{k+1}} r_b^{k+1} \right) \quad (k = 1, 2, 3, \dots, n-1) \quad (4)$$

and for  $k = n$ , we have

$$r_b^n = p_{0,e}^n + 0.75 p_{1,n}^n + 0.75 p_{1,b}^n$$

at the last stage of the switch. It is noted that  $r_n^n$  and  $r_b^n$  have the same expression. This is because at the last stage of the switch, the probability that the buffer at the next stage can accept a packet is always 1.

As mentioned before,  $q^k$  is defined as the steady state probability that a packet is ready to come to a buffer of an SE at stage  $k$ . This probability is given as follows:

$$q^k = 0.75(1-p_{0,e}^{k-1})(1-p_{0,e}^{k-1}) + 0.5p_{0,e}^{k-1}(1-p_{0,e}^{k-1}) + 0.5(1-p_{0,e}^{k-1})p_{0,e}^{k-1} \quad (k = 2, 3, 4, \dots, n) \quad (5)$$

Also notice that  $q^1$  is the input load of the switching fabrics.

With the above discussions, a recursive algorithm can be formed to calculate the steady state probabilities of the buffered Banyan switch at each stage.

##### Performance Parameters Formulations

In the performance analysis of the single buffered Banyan switching fabric, three important parameters are considered. They are network throughput, network delay and the delay variance.

1) **Network Throughput.** Let  $\lambda^k$  be the throughput per port at stage k of the network. We define

$$\lambda^n = p_{1,n}^n r_n^n + p_{1,b}^n r_b^n \quad (6)$$

as the normalized network throughput, where  $n$  is the number of stages of the Banyan switch. Notice that at the last stage of the switching network,  $q^{n+1}$  is equivalent to  $\lambda^n$ .

2) **Network Delay.** The network delay is defined to be the average clock cycles required to transmit a packet across the Banyan network. Here we use the normalized delay as the mean delay at one stage of the Banyan network.

$$d = \frac{1}{n} \sum_{k=1}^n \left( 1 + \frac{1-r_n^k}{r_b^k} \right) \quad (7)$$

Detailed derivation of  $d$  can be found in Appendix A.

3) **The Variance of Delay.** In the performance analysis of ATM switching fabrics, the variance of the switch delay is an important parameter. In this paper, we use the moment generation function to derive a closed form expression for the variance of the delay. The normalized standard deviation of the network delay can be shown (see Appendix B) as follows:

$$\sigma = \frac{1}{n} \sum_{k=1}^n \sqrt{\frac{(1-r_b^k) + r_n^k (r_b^k - r_n^k)}{(r_b^k)^2}} \quad (8)$$

## Performance Results and Comparisons

Performance results in comparison with the previous "two-state" model by Jenq [4] and Yoon [6] are plotted in Fig. 3 - Fig. 5. These figures include plots for both the two state model and the three-state model at various number of stages, i.e.  $n=1, 2, 4, 6, 10$ .

In Fig. 3, normalized throughput vs. input load  $q^1$  are plotted at various switch sizes. It is seen from the results plots that for Banyan switch of small size, the "three-state" model has nearly the same throughput as the "two-state" model. But as the number of stages goes beyond 4, there is significant difference in throughput between the two models. As was pointed out by Yoon [6], the analytic results of the "two state" model are more optimistic than

simulation results. For a single buffered Banyan network with stage  $n = 6$ , at input load  $q^1 = 1.0$ , the analytic throughput is about 49% while the throughput from simulation result is about 40%. The analytic throughput of the "three-state" model under the same network condition is 42%, which is much closer to the simulation result than the previous model. Therefore, the newly proposed "three-state" model gives more accurate prediction for the performance evaluation of the switching fabric. It is shown from Fig. 3 that as input load  $q^1$  approaches to 1.0, the normalized throughput tends to converge to an asymptotic value of 36% for (1024x1024) Banyan switch.

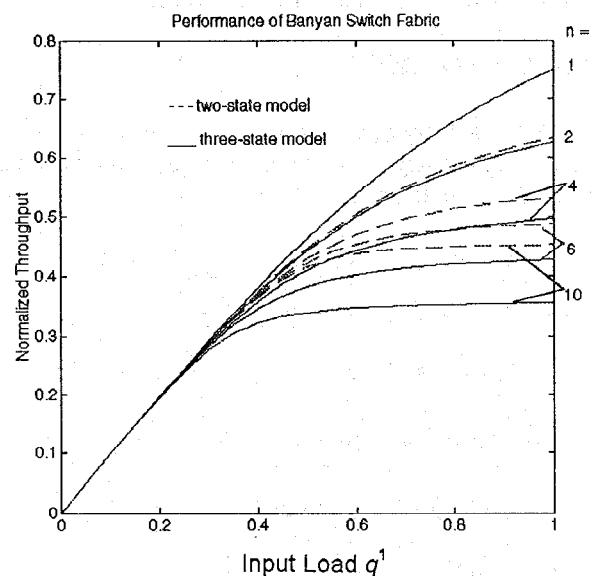


Fig. 3 Normalized Throughput versus Input Load

The normalized network delays for various network sizes are plotted versus input load in Fig. 4. Again, for small size network, there is not much difference in delay between the two models. However, as the network size increases to beyond 6, there is some noticeable difference in delay between the two models. The "two-state" model tend to have more optimistic results. For  $n = 6$ , the normalized delay of the "three-state" model is about 1.55 clock cycles with input load equal to 1.0. The normalized delay of "two-state" model under same network condition is about 1.51 clock cycles. It can be seen from the plot that switch with large size tend to have longer delay. This is due to the fact that for blocking switch, contention will occur more often in larger network and therefore results in a higher network delay. Also notice that for

small size switch, the delay increases almost linearly with input load.

The normalized standard deviation of the network delays for various network sizes are plotted vs. input load in Fig. 5. There is a significant difference in the standard deviation of delays between the two models. Again, the “two-state” model tend to have more optimistic results. This is due to the fact that a blocked packet will assume the same output port of an SE at the next clock cycle is not considered in the “two-state” model. For  $n = 6$ , the normalized standard deviation of the delay for the “three-state” model is about 1 clock cycle with input load equal to 1.0. The normalized standard deviation of the delay for the “two-state” model under same network condition is about 0.86 clock cycles. It can be seen from the plot that larger network tend to have higher delay variation.

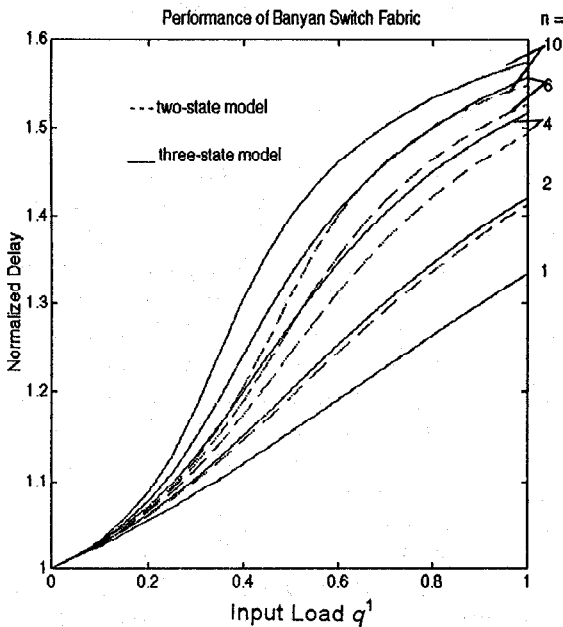


Fig. 4 Normalized Network Delay versus Input Load

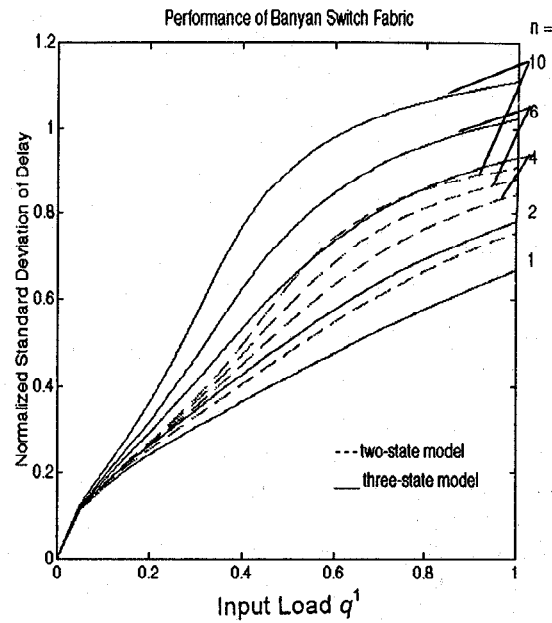


Fig. 5 Normalized Standard Deviation of Network Delay vs. Input Load

## V. Performance Analysis of the ATM Switching Fabric With Packet Priority

### The Packet Priority Scheme

Since Banyan based ATM switches are internally blocking switches, contention occurs when two packets in different buffers within the same switching element are going to the same output port of that SE. The ATM switching fabric described in the previous sections resolves the contention by choosing at random one of the two contending packets regardless of whether the packet has been blocked before or not. Under this routing algorithm, if a packet that has been blocked in the previous clock cycle happens to be not chosen to move forward to the next stage at the current clock cycle, it will experience more delay than a “new” packet which is chosen to move forward at the current clock cycle. This tends to enlarge the variation of the network delay. For delay sensitive services like audio and video supported by ATM, we wish to reduce the variance of the delay as much as possible. In this section, we introduce a new routing scheme by giving the “blocked” packet higher priority to move forward when it is contending with a “new” packet. In case when two contending packets are of the same type, i.e. both are “new” or “blocked”, one is chosen at random by the routing logic to move forward. With this new scheme, we expect that the variance of the network delay will be reduced.

With the introduction of the routing priority scheme for the blocked packet during contention, the first term in equation (4) for  $r_n^k$  needs to be modified, i.e., the probability that a “new” packet is ready to move forward is

$$p_{0,e}^k + 0.75 p_{1,n}^k + 0.5 p_{1,b}^k$$

Therefore, we have the modified expression for  $r_n^k$

$$r_n^k = (p_{0,e}^k + 0.75 p_{1,n}^k + 0.5 p_{1,b}^k) \cdot (p_{0,e}^{k+1} + p_{1,n}^{k+1} r_n^{k+1} + p_{1,b}^{k+1} r_b^{k+1})$$

( $k = 1, 2, 3, \dots, n-1$ )

(9)

and for  $k = n$ , we have

$$r_n^n = p_{0,e}^n + 0.75 p_{1,n}^n + 0.5 p_{1,b}^n$$

at the last stage of the switching network.

Similarly, we have a modified expression for  $r_b^k$

$$r_b^k = (p_{0,e}^k + 0.75 p_{1,b}^k + p_{1,n}^k) \left( \frac{p_{1,n}^{k+1}}{p_{1,n}^{k+1} + p_{1,b}^{k+1}} r_n^{k+1} + \frac{p_{1,b}^{k+1}}{p_{1,n}^{k+1} + p_{1,b}^{k+1}} r_b^{k+1} \right)$$

( $k = 1, 2, 3, \dots, n-1$ )

(10)

and for  $k = n$ , we have

$$r_b^n = p_{0,e}^n + 0.75 p_{1,b}^n + p_{1,n}^n$$

at the last stage of the switching network.

### A Variable Priority Probability

In the above discussion, we assume that when contention occurs between a “blocked” packet and a “new” packet, the “blocked” packet will have the priority of being chosen to move forward (with priority probability = 1). It is interesting to see how the switch performance, especially the variation of the delay, is affected when the degree of packet priority varies. To do this, let's introduce a variable priority probability  $P$  to the Banyan switch's routing control scheme.

$P$  = the probability that a “blocked” packet is chosen to move forward when it is contending with a “new” packet.

The value of  $P$  can vary from 0 to 1. When  $P = 1$ , it is the case studied above. When  $P = 0.5$ , there is no packet priority. This corresponds to the situation described in Section IV. When  $P = 0$ , the “new” packet will be chosen with higher priority to move forward when it is contending with the “blocked” packet. We expect that the variance of the switch delay will decrease as  $P$  goes from 0 to 1.

With the introduction of this probability  $P$ , the expressions for  $r_n^k$  and  $r_b^k$  are therefore adjusted as follows:

$$r_n^k = [p_{0,e}^k + 0.75 p_{1,n}^k + 0.5 p_{1,b}^k + 0.5(1-P) p_{1,b}^k] \cdot (p_{0,e}^{k+1} + p_{1,n}^{k+1} r_n^{k+1} + p_{1,b}^{k+1} r_b^{k+1}) \quad (11)$$

where the term  $0.5(1-P) p_{1,b}^k$  is coming from the event that both the “new” and “blocked” packets are going to the same output port but the “new” packet is chosen to move forward, and

$$r_b^k = (p_{0,e}^k + 0.75 p_{1,b}^k + 0.5 p_{1,n}^k + 0.5 P \cdot p_{1,n}^k) \left( \frac{p_{1,n}^{k+1}}{p_{1,n}^{k+1} + p_{1,b}^{k+1}} r_n^{k+1} + \frac{p_{1,b}^{k+1}}{p_{1,n}^{k+1} + p_{1,b}^{k+1}} r_b^{k+1} \right)$$

(12)

where the term  $0.5 P \cdot p_{1,n}^k$  is coming from the event that both the “blocked” and “new” packets are destined to the same output port but the “blocked” packet is chosen to move forward.

The remaining part of the analysis including the formulation of the switch performance parameters remains the same as that in Section IV. In a similar fashion, a recursive algorithm can be formed to calculate the probabilities in the model with packet priority and the performance parameters.

### Performance Results and Comparisons

Performance results of the “three-state” model with packet priority are plotted in Fig. 6 - Fig. 8. The switch performance including throughput, delay and standard deviation of delay versus input load are plotted in Fig. 6 for both  $P = 1.0$  and  $P = 0.5$ . The switch has  $n = 6$  stages. When the switch input load equals to 1.0 and  $P = 1.0$ , the normalized throughput is about 48%; the normalized network delay is about 1.5 clock cycles; the standard deviation of the delay is about 0.74 clock cycle. In the case of no packet priority ( $P = 0.5$ ), at input load equals to 1.0, the normalized throughput is about 42%; the normalized network delay is about 1.55 clock cycles; the standard deviation of the delay is about 1.05 clock cycles. In comparison with the switch without packet priority, the one with packet priority given to “blocked” packet has better performances at various input loads.

In order to show how network performance especially the variance of the network delay is affected by the packet priority probability, the performance of the network versus  $P$  is plotted in Fig. 7 with input load  $q^1 = 1$  and  $n = 6$ . The performance results show that as the packet priority probability increases from 0 to 1, the variance of the delay decreases significantly. At input load equal to 1.0, the standard deviation of the network delay decreases almost linearly with the increase of  $P$ . There is an approximate 35% reduction in standard deviation of the delay when  $P$

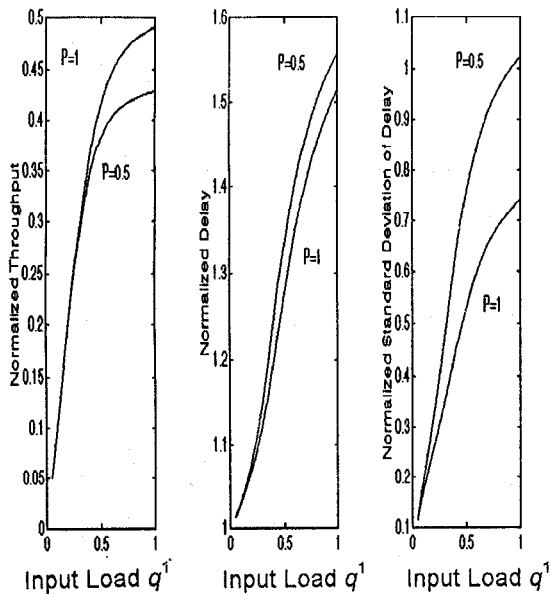


Fig. 6 Network Performance versus Input Load at  $n = 6$

goes from 0.5 to 1. Also it is interesting and delighting to notice that the other two performance parameters, throughput and delay are also improved (almost linearly) when  $P$  increases. The throughput is improved by about 10% as  $P$  goes from 0.5 to 1. When  $P = 0$ , this corresponds to the case when the “new” packet will always be given higher priority to be moved forward when it is contending with a packet that has been blocked before. In this the case, the switch has the largest delay variance. As  $P$  goes from 0 to 1, the likelihood for a blocked packet to be moved forward is increased, therefore reduce the delay variation between the “blocked” packets and “new” packets. Also, as  $P$  increases, those paths in the switch that are blocking the packets will be off loaded and hence reduce the switch delay and improve the throughput.

The performance results in Fig. 6 and Fig. 7 confirm our earlier conjecture that by introducing the packet priority probability, the variance of the network delay is indeed reduced and also the throughput and delay are improved. Also in Fig. 7, we show a recently obtained simulation result from [15] for comparison with the analytical results. It is seen that the analytical results are still more optimistic. The simulation results show that as the packet priority probability increases from 0.5 to 1, there is only a slight improvement in throughput and delay while an approximate 22% reduction in the standard deviation of delay.

In order to see the asymptotic character of the network performance, plots of the normalized throughput with  $P=1.0$  and  $P=0.5$  versus network size  $n$  is shown in Fig.

8. It is seen that with input load equal to 1.0, as the network size increases the normalized throughput approaches to about 35% for the “three-state” model with packet priority probability equals to 1.0. In the case of no packet priority ( $P=0.5$ ), the normalized throughput approaches to about 28%. Again it is shown that the throughput is improved when using the packet priority.

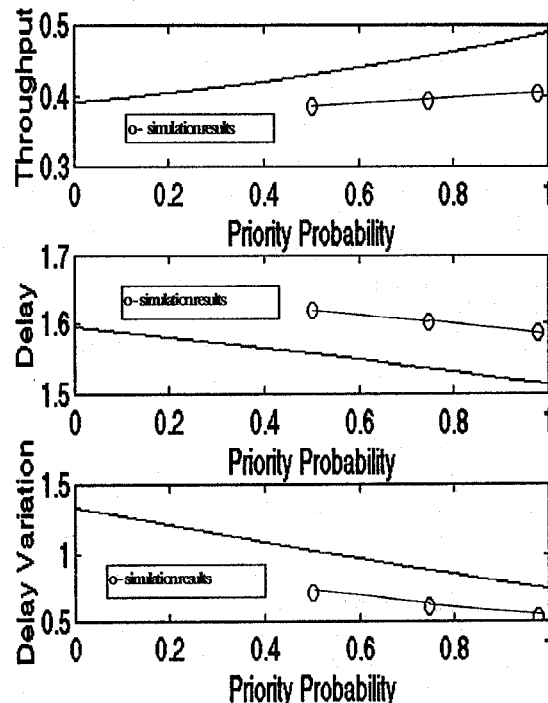


Fig. 7 Network Performance versus Packet Priority Probability at  $n = 6, q^1 = 1.0$

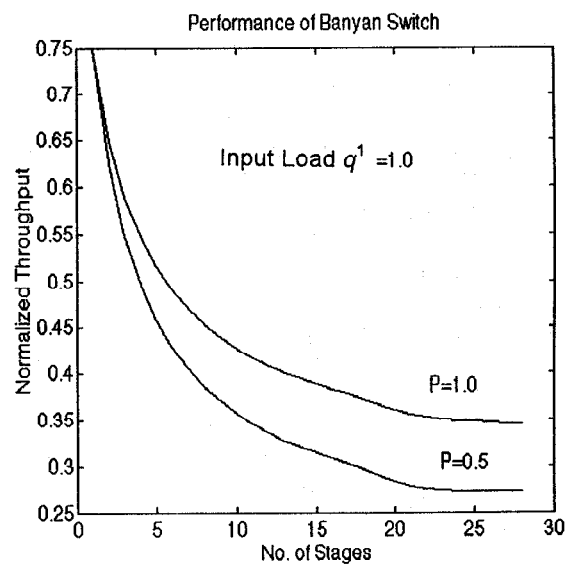


Fig. 8 Normalized Throughput versus Network Size  $n$

## VI. Conclusion

In this paper, we propose a new model for the performance analysis of an ATM switching fabric based on single-buffered Banyan network. In this new model, we describe the behavior of the switching element in the Banyan network by introducing a third state into the Markov chain model to deal with the situation that a blocked packet will still destine the same output port in the next clock cycle. The proposed model is shown to be more accurate in evaluating the performance of the Banyan switch than the "two-state" model.

A simple priority scheme to deal with contention in the switching element is investigated in the proposed ATM switching fabric by giving the "blocked" packet higher priority to move forward to the next stage when it is competing with a "new" packet. For a fully loaded six-stage switch, the analytical results show that the delay variation can be reduced by 35%, while the simulation shows a 22% reduction.

The analytical model developed in this paper can be extended to analyze the Banyan network with multibuffer and switching element with arbitrary size. The traffic pattern that we used for the performance analysis in this paper is uniform. However, for more realistic ATM environment, the study of the performance of the proposed "three-state" ATM switching fabric with packet priority under nonuniform traffic is still needed.

## Appendix

### A. Derivation of the Mean Delay

Consider the probability distribution of the delay which is a discrete random variable. Let  $p_i$  be the probability that the delay at stage  $k$  is  $i$  clock cycle(s). Therefore, we have

$$p_i = r_b^k (1 - r_b^k)^{i-2} (1 - r_n^k) \quad (i = 2, 3, 4, \dots)$$

and  $p_1 = r_n^k$

Let  $P(z)$  be the moment generating function of the delay. Thus

$$\begin{aligned} P(z) &= \sum_{k=0}^{\infty} p_k z^k \\ &= p_1 z + p_2 z^2 + p_3 z^3 + p_4 z^4 + \dots \\ &= r_n^k z + (1 - r_n^k) r_b^k z^2 + (1 - r_n^k)(1 - r_b^k) r_b^k z^3 + (1 - r_n^k)(1 - r_b^k)^2 r_b^k z^4 + \dots \end{aligned}$$

$$\begin{aligned} &= z \{ r_n^k + (1 - r_n^k) [ r_b^k z + (1 - r_b^k) z^2 + (1 - r_b^k)^2 z^3 + \dots ] \} \\ &= z \left\{ r_n^k + \frac{(1 - r_n^k) r_b^k z}{1 - (1 - r_b^k) z} \right\} \end{aligned} \quad (A.1)$$

Take the first derivative of (A.1), we have

$$P'(z) = r_n^k + (1 - r_n^k) r_b^k z \left\{ \frac{1}{1 - (1 - r_b^k) z} + \frac{1}{[1 - (1 - r_b^k) z]^2} \right\} \quad (A.2)$$

Therefore, the mean delay at stage  $k$ ,  $d(k)$  is expressed as follows:

$$\begin{aligned} d(k) &= P'(1) \\ &= r_n^k + (1 - r_n^k) r_b^k \left\{ \frac{1}{1 - (1 - r_b^k)} + \frac{1}{[1 - (1 - r_b^k)]^2} \right\} \\ &= r_n^k + (1 - r_n^k) \left( 1 + \frac{1}{r_b^k} \right) \\ &= 1 + \frac{1 - r_n^k}{r_b^k} \end{aligned} \quad (A.3)$$

### B. Derivation of the Delay Variance

From (A.2) we have the second moment

$$P''(z) = (1 - r_n^k) r_b^k \left\{ \frac{1}{1 - (1 - r_b^k) z} + \frac{1}{[1 - (1 - r_b^k) z]^2} \right\} + z(1 - r_b^k) \left\{ \frac{1}{[1 - (1 - r_b^k) z]^2} + \frac{1}{[1 - (1 - r_b^k) z]^3} \right\} \quad (B.1)$$

Therefore,

$$P''(1) = \frac{2(1 - r_n^k)}{(r_b^k)^2} \quad (B.2)$$

Hence the variance of the delay at stage  $k$  is

$$\begin{aligned} \text{Var}\{delay(k)\} &= E \{ \{delay(k) - E[delay(k)]\}^2 \} \\ &= E \{ \{delay(k) - d(k)\}^2 \} \\ &= E \{ [delay(k)]^2 \} - d^2(k) \\ &= P''(1) + P'(1) - [P'(1)]^2 \\ &= \frac{2(1 - r_n^k)}{(r_b^k)^2} + \frac{1 + r_b^k - r_n^k}{r_b^k} + \frac{(1 + r_b^k - r_n^k)^2}{(r_b^k)^2} \\ &= \frac{(1 - r_b^k) + r_n^k (r_b^k - r_n^k)}{(r_b^k)^2} \end{aligned} \quad (B.3)$$

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