

# DFM – A Fabless Perspective

Jitendra B. Khare

Ample Communications, Inc. Fremont, CA USA

## Abstract

*The fabless model has proven immensely successful for IC companies over the last decade. However, at smaller geometries, process-design interactions are causing design marginality and reliability failures. This paper argues that systematic application of DFM techniques is needed in fabless companies to reduce such (potentially catastrophic) failures.*

As IC manufacturing technology shifts to 0.13um and below, process-design interactions are becoming very complex. On-chip process variations, pattern-dependent failures, increased via failure rate, etc. are making it harder to separate the process from design using “simplified” design rules. In addition, process ramps have become longer, forcing designs into not-so-stable processes. Such a paradigm is new for engineers in fabless companies, who have traditionally been isolated from the process through the interface of design rules and process corners. As a result, an increasing number of SoCs are being designed by fabless companies without understanding the process-design interaction, resulting in chips that are, in some cases, process-marginal. These marginal designs yield very poorly and decrease the company’s competitiveness, causing loss of profits and markets. In addition, they can have higher test escapes, leading to larger test cost and/or lower reliability. To alleviate these problems, the use of DFM is becoming an increasing necessity in newer processes.

Traditionally, fabless designs are a mixture of soft/hard IPs, some custom design, and mostly APR-driven layout. The dominant IPs used are standard cells and memories (RAMs, register files and ROMs). It has been shown that DFM-oriented standard cell designs can improve yield by as much as 5-6%. Similar improvements can be achieved for memories. For larger memories, compilers with built-in redundancy can also increase yield substantially. IP vendors, therefore, have an important DFM role, which should be emphasized by the fabless companies.

However, more dramatic results can be achieved by applying DFM to all aspects of the SoC design. DFM

should start at the system design stage itself. For example, cost trade-offs can be made between single chip SoCs and MCMs. We have seen yield/cost improvements of more than 30% using this approach. Similarly, the chip architecture itself can be optimized for yield. For example, building architectural redundancy into large memory arrays (configured using BIST on power up) can not only improve yield substantially, but can also save the cost of expensive redundant-memory compilers and laser repair. Design techniques, such as design centering for analog macros, and avoiding extensive use of global clocks can also improve yield.

Significant yield savings can be achieved in the layout stage as well. Traditionally, design rules provided by foundries are based more on process capabilities than on yield analysis. In typical APR designs, higher metal (metal 3 and above) utilization is less than optimal. Hence, the design rules for these metals can be relaxed without increasing die area. Such methods can lead to more than 25% yield improvement. Other techniques, such as statistical double via insertion can also be used to improve yield.

Any DFM strategy for fabless companies cannot be separated from the extensive usage of Design for Test (DFT) and Design for Debug (DFD) methods. For DFM techniques to work, defect and process variation data must be known. However, foundries are willing to provide rudimentary data, at best. Hence, fabless companies have to extract this data from their own defective chips. This can be achieved only through the proper use of DFT/DFD. Using these techniques, defect data can be extracted from both memory and the logic portions of the die. In addition, comprehensive DFT techniques are needed for both system-level DFM (e.g. known good die in an MCM) and architectural DFM (BIST).

In conclusion, as chip features shrink, design engineers need to end the design/process isolation and understand the manufacturing process. Fabless companies will be able to keep building successful SoCs only by implementing a sound DFM strategy, coupled with DFT/DFD methods.

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