

# Managing the Multi-Gbit/s Test Challenges

Ulrich Schoettmer, Bernd Laquai  
Agilent Technologies, Boeblingen

CMOS technology continues to evolve following Moore's law enabling new levels of integration, performance and cost. Within a fairly short period of time we will see a pretty significant architectural transformation within desktop computers, servers, laptops, and even in your digital entertainment center:

The multi-drop buses transform into an on-board packet switched network connecting high-performance chips with differential high-speed point-to-point links. Serial ATA is leading the pack, PCI-Express is emerging, just to name a few, they will soon be common-place to the PC industry. Chipsets in the computation and consumer space are under severe cost pressure, which creates a severe challenge to the traditional test strategies.

Structural test methodologies and associated development tools have emerged and provide a notion of: As soon as everything is synthesized digitally, there is no need for big iron ATE anymore. So while the ATE industry is squeezing to provide ever more economic solutions there is a raising concern as to how to ECONOMICALLY MANUFACTURE gigabit links without biting into \$ margins.

Low cost loop back (internal and external via piece of wire) has been the credo to cover serial link technology for low and high-end applications but: How do I deliver good quality and compliance to standards based on this minimalistic approach? How do I manage to identify process marginality, which becomes a growing concern as we move forward to nanometer technology? What tells me that low jitter PLLs, equalization and the jitter tolerant data recovery unit are intact? The loop may work, so does the application?

On the other hand the DFT enabled (wire) loop has some great advantages over conventional pre-stored pattern test approaches as it relieves the test pattern generation and debug process from ATE. It runs at native speeds, provides protocol independent link synchronization and is able to deal with latency variation and non-deterministic packet sequences easily.

The logical step towards an ECONOMIC breakthrough in HVM is to take advantage of those things which can be done right on the silicon with digital design tool support and have the ATE focus on the parametric side of the test challenges. This leads to the new concept of parameterized loop back technology integrated into ATE.

This new concept fills the parametric fault coverage gap of the simple wire loop by adding the capability of jitter and sensitivity tests with the ATE acting as external precision reference. The additional DC parametric test access rounds up the picture. Significant cost drivers like precision timing and formatting as well as pattern generation and compare circuitry are eliminated. So what you finally get is a solution based on easy to synthesize DFT, focussing ATE onto what is hard to achieve timely enough with on-chip instrumentation.

The parameterized loop back concept can provide high coverage over a wide technology range with high port counts at very attractive price points, which results in a superior cost of test equation.

Characterization though will be ever more challenging, as low cost HVM has to rely on a more thorough validation of design robustness. The most promising approach in terms of economics is to characterize "pars pro toto" or a piece for a whole and to apply a hybrid test solution based on ATE plus leading edge rack and stack instrumentation. This gives the opportunity to leverage equipment used for system validation and debug, providing the ultimate performance metrics and the thoroughness of analysis you need to do prior to lunch HVM.

In summary: The synergy between DFT and ATE appears to be the only way to reach the economical goals for HVM. The parameterized loop back is just the implementation of this learning. On the other side, the convergent use of bench equipment for system level test and for device characterization on hybrid ATE is the other logical step to go.