

Cost Containment for High-Volume Test of Multi-GB/s Ports

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Minimize Expensive Analog Test Solutions

The agenda of high volume manufacturing (HVM) test is cost. Equipment costs, throughput, factory overhead, yield, and many other parameters make up overall test costs. But the start of any cost optimization must start with a very clear perspective of what HVM test must achieve, and what it cannot afford to be responsible for. HVM test is mostly a screen to ensure that outgoing products meet established goals for quality defect rate and reliability. It cannot afford to duplicate design validation processes that do not efficiently support this primary screening goal. Multi-GB/s devices drive this distinction to a critical level.

Testing the analog attributes of multi-GB/s in a native capacity is expensive. Compare the digital vs analog capabilities for typical digital testers in various speed categories.

Data Rate ->	<1GB/s	1-2GB/s	2-6GB/s
Analog Cost Drivers			
Pin Driver	Off-the-shelf, 400-650ps Tr	Custom 200ps Tr	Custom LVDS
Compare BW	<2GHz	<4GHz	>10GHz
Tooling Connection	I/O bi-dir, single-ended, pogo	I/O bi-dir, single-ended, fly-by, pogo	Differential, coax
Accuracy	100ps	50-75ps	<40ps p-p
Features	PPMU	Source sync output latching	Jitter, BER, DM, CM testing, protocol matching
Digital Cost Drivers			
Pattern, Formatters,	Complex pattern formatting, data source selection, APG, time set switching	Deep data capture and post-process	Deep pattern memory (>1G)

It is apparent the complexity in the slower applications is embedded in digital areas that are proceeding nicely down the integration cost curve (\$100's per channel). As speed increases, the technical challenge moves from digital issues to physical/electrical. Here, cost effective solutions for high performance circuits and interfaces are not progressing so well (\$1000's per channel).

While we need to establish high data rate test solutions, we cannot chase physical/electrical layer performance testing in HVM. More specifically, we need fast data rates but we cannot expect an HVM tester to replicate or test for adherence to an end-use electrical environment that is increasingly different from a practical ATE test socket.

What Do We Need To Test?

Our HVM test screens need to best fit these criteria:

1. Expose a population of device defects that account for the required out-going quality level goals.
2. Require the lowest cost equipment and tooling
3. Execute in the shortest period of time.
4. Provide adequate process feedback.
5. Can be developed and sustained within reasonable cost and schedule.

Our industry has driven these items via numerous initiatives that involve ATE cost reductions (including structural test platforms), device DFT (including BIST), test methods sharing and re-use, HVM process refinement, test time reduction methods, and many others. For digital devices incorporating high-speed ports, the same principles are being applied.

Do we need to directly validate the high-speed port specification via direct interface to test instruments in HVM? The answer had better be NO! Why? Because it is most likely not possible – and better interface defect screening capability exists within the device's own DFT potential than an external connection could provide. DFT-enabled internal circuits that use variation matching (vs external measurement accuracy) should be the basis for electrical interface defect screening. Other topics at this conference explore these approaches in detail.

The device 'core' and other aspects of the device still require the tester to apply functional test screens as well as manipulate DFT-based screens. Test pattern stimulus and response through high-speed interfaces may work at a lower speed; however, there are good reasons to maintain high interface data rates. First, the number of test vectors that need to be applied as we march toward the billion-transistor device stresses test time. Second, design optimization, performance, and test defect coverage can be compromised if the device core must allow for 'data starvation' during test.

Directions

We need to execute stored stimulus/response test patterns via high-speed interfaces at native rates. Native-mode output testing is more challenging because clock recovery and device non-determinism are significant obstacles. Device DFT and test pattern content will have to converge to either replicate or suspend at-speed protocol-based native mode non-determinism. Can we afford to directly strobe output response cycle-by-cycle? NO! Device DFT must manage at-speed response capture during HVM test. Current production solutions demonstrate this approach and open the door for reduced support, and associated tester costs, for logic output pin testing at high data rates.

One thing is clear. HVM cannot afford the cost of replicating and directly testing end-use specifications for physical layer electrical properties of multi-GB/s DUT ports.

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