Open Architecture ATE and 250 Consecutive UIs

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1. Problem Statement and Data Recovery Architecture

Problem Statement. A very different way is needed to perform jitter testing of multi-Gbps physical layer ICs on a high-volume production line [1]. To perform high-volume production testing, several issues must be addressed. First, what measurements are required to characterize jitter in multi-Gbps physical layer ICs? Should the BER performance of the IC be tested or not?

Secondly, as shown in Figure 1, the PCI Express standard defines an eye diagram test for receivers (R_X) [2]. Is an oscilloscope sufficient for production test with respect to a test time and the required accuracy of BER < 10^{-12}? In fact, the data recovery architecture which is implemented in the IC under test should determine the type of measurements required.

Which Architecture? In a multi-Gbps physical layer IC, the key measurement is the timing misalignment between an incoming bit sequence and a sampling clock. It follows that edge fluctuations in the bit sequence and the clock should be measured.

Is a jitter tolerance test required? If the IC implements data recovery by combining a phase detector and a charge pump to provide integrated sampling phase error to a VCO, the answer is *yes*. Due to the PLL-dependent architecture, it requires a jitter tolerance test. However, the less the BER threshold becomes, the longer the test time it requires. Thus, its test time prevents it from being used in the production line. Instead, a new method is required and one was proposed, which can perform the test with a 10X reduction in test time [3].

On the other hand, if the IC recovers data by oversampling each serial bit using sampling clocks provided from a VCO, with the sampling frequency controlled by an external reference clock, the answer is *no*. Since the oversampling provides *M* samples of each bit, the timing misalignment between a bit sequence and an oversampling clock is relaxed and jitter is reduced to the random jitter associated with the bit stream. In this case, it is sufficient to measure the RMS value of the input timing jitter at the R_X package pins.

2. Open Architecture ATE Breaks Test Barriers

An Oscilloscope or More? What are the available options for reducing the equipment cost? Some specifications require a timing jitter measurement using *250 consecutive UI in the center of a 3500-UI pattern* [2]. This exceeds the capabilities of a TIA or a sampling oscilloscope. At least a real-time oscilloscope is required to meet this specification. Although oscilloscopes of 20 GS/s capability are commercially available, the required accuracy of jitter measurements satisfying a maximum BER of 10^{-12} in addition to an allocated test time < *200 msec* imposes a significant testing barrier to these oscilloscopes.

To meet this jitter tolerance testing challenge, an open architecture ATE, that combines a real-time oscilloscope with the sophisticated jitter measurement algorithm like the $\Delta\phi$ method [1], [3], can simultaneously break the test time, equipment cost and accuracy barriers. Furthermore, it has been demonstrated that the $\Delta\phi$ method provides results that are almost perfectly compatible with TIA and BERTS [3]. Also, since the same system can be used for both R&D and production testing, the transition time required to establish a good correlation between production and R&D measurements is shortened.

3. Summary

The combination of external test resources, such as 20 GS/s real-time oscilloscopes and the $\Delta\phi$ method, under the open architecture ATE can meet the challenge of testing PCI Express physical layer ICs.

Acknowledgement

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References

[1] T. J. Yamaguchi, "Multi-GHz Interface Devices Should be Tested Using External Test Resources," in *Proc. IEEE International Test Conference*, Baltimore, MD, Oct. 7-10, 2002, pp. 1229.

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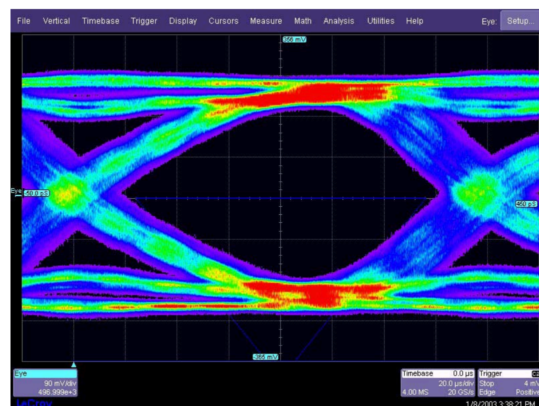

Figure 1. Eye Diagram of PCI Express IC.

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