

Production Test Challenges And Possible Solutions For Multiple GB/s ICs

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As the data rate reaches 1 Gb/s or beyond, most of the communication standards use the serial link architecture due to its capability of delivering data at a rate up to 100 Gb/s and beyond. This serial link is an asynchronized system with a bit clock embedded in the transmitting data bit stream. Transmitting multiple Gb/s data for a single channel over a distance of $\sim 10 \text{ m} < L < \text{a few } 1000 \text{ km}$ are all serial, with standard examples of Giga Bit Ethernet (GBE), Fibre Channel (FC), and SONET. The transmitter, receiver, and transceiver ICs for those communication links are characterized by fiber medium, high cost, low volume, and limited integration in comparison with the mainstream commodity ICs. The production test for those ICs are often conducted with rack-and-stack of certain lab instruments, or some home-grown testers, resulting in a high cost, low throughput test solution. Such a production test solution is not favored, but may still be justifiable given the mean high unit sale price for those ICs ($> \$1000/\text{device}$).

Meanwhile, the chip-to-chip ($L < 1 \text{ m}$) communication link in the PC peripherals has evolved from architectures of globe clock, to source synchronized, and to serial link as data rate increased from $\sim 200 \text{ Mb/s}$ for globe clock to $> 1 \text{ Gb/s}$ for serial link. The transmitter, receiver, and transceiver ICs for backplane I/O links are characterized by copper medium, low cost, high volume, multiple channels, and significant integration. Typical standards for copper based serial communication include: PCI-Express, Infiniband, Serial ATA, Rapid IO. The high volume and low cost can be put in perspective by the ~ 2 billion PCI Express ports on the chipset in a PC expected to be shipped in the first year of its production, and this number is much larger than the sum of all the Gb/s ports shipped so far for fiber based datacom and telecom applications. Testing those ICs in production is expected to encounter three major difficulties of : a.) the instrument rack-and-stack approach developed for datacom and telecom ICs will no longer be a viable solution due to its high cost and slow test time; b.) traditional ATEs are synchronized system with a distributed globe clock and do not fit into the asynchronized serial link scheme well; c.) new analog/mixed-signal parameters/functions of timing jitter, amplitude noise, eye-diagram, and bit error rate (BER) required for serial link are not offered by most ATEs with necessary accuracy at multiple Gb/s rate.

It is believed that no single company along can solve all those challenges. To discuss the possible solutions in dealing with those challenges identified, a panel consists of leading experts from leading companies and academia across the technical fields of IC design and manufacture, instrumentation, and ATE is formed. Outstanding questions discussed by this panel for the multiple Gb/s serial link will include, but not limited to : a.) what need to be tested in production and why? b.) what will be the viable test method: ATE, or open architecture (OA) with module instruments, or DFT/BIST, or combination between them? c.) what are the bandwidth, DJ, RJ, and noise requirements for the tester hardware and how to verify them? d.) what constitute a correct jitter/signal integrity testing method? e.) how can we test BER down to 10^{-12} within seconds?

Moderator: David Keezer, Georgia Institute of Technology

Panelists: Yi Cai, Agere
John Johnson, Intel
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