

Diagnosis in Modern Design – Just the Tip of the Iceberg

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In today's world of efficiency and productivity, time to "something" is always critical. Here, the functional design or artwork release is typically not the product. The product is done pretty much when the customers have it in their hands – and that is after turn-on and volume ramp.

The people who practice the crafty arts of diagnosis & debug work against an unforgiving timeline as they hack together tools and techniques to determine problems hidden in hard silicon, systems or processes.

When test is done right, that is to an acceptable quality specification (and without impeding productivity and cost), defective parts fail the screening process. Without splitting hairs on definition, diagnosis and debug digs deeper to determine why the part is unacceptable. Troubleshooting how and why a part (or system) fails is important. For example, this may be needed for yield improvement, process monitoring, debugging the design function, failure mode learning for R&D, or just getting a working first prototype. But the detective work can become tricky. One reason for this is that, while many segments of the product creation flow (e.g. the design and test development flows) have benefited from years of study and automation, diagnosis has somewhat lagged in the formalization of techniques. Also, the test floor equipment have been traditionally designed and operated for pass/fail oriented testing. Unless this situation improves, an *effective* diagnosis-friendly environment may be elusive when it is needed most.

Analysis software and equipment operation for diagnosis are opportunities. Sometimes, another issue is accountability – especially during turn-on. For example, in many modern "disaggregated supply chain" designs, circuit blocks, libraries, engineering and fabrication services may be acquired from different sources, standard libraries may have been modified, and test-chip data or design models may not correlate well with process parameters at-volume. Ultimately (and sometimes unfortunately) the chip supplier is responsible for delivering on-time, and thus ends up owning the problem. And yes – some bugs just remain unsolved.

The panel of test & diagnosis experts will describe their experiences and best practices. They will also discuss the opportunities for development and contribution in the ATE, EDA and R&D fields.

Organizer: Fidel Muradali – Agilent Technologies
Moderator: Mike Ricchetti - Intellitech

Panelists: Wu-Tung Cheng – Mentor Graphics
Bruce Cory - Nvidia
Bill Huott - IBM
Bernd Koenemann - Cadence
Robert Molyneaux – Sun Microsystems

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