

ATE-Customer Perspectives & Requirements Panel

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Historically ATE tracked the performance and interface characteristics of the devices being tested. Over the past decade, the cost of pursuing this path has is becoming prohibitive and DFT has entered to address this issue. The “right” balance of test on and off the chip has been a source of considerable discussion since DFT made its entrance into the equation.

Does one do the “minimum” DFT just to avoid buying the “next” tester, does one do all the test “on chip” and cost reduce the ATE down to a battery and a data source and sink, or is silicon so precious that any use for non mission related function make the cost of the final die prohibitive. One can easily find proponents for each position and the data to back it up. This is because the answer is highly dependent on the particulars of the design of the device and the issues related to the business case that the device is going into.

So, how does one address this with the architecture of the ATE. Flexibility is still an important factor in the equation. The architecture needs to be able to be configured to meet the demands of the particular business it is applied into. Function and performance still need to be options that can be selected, once size does not fit all situations. Certainly the options may include the performance level of the I/O's and the analog. Pin count options can be utilized either for large devices or for

high parallelism. Specialized function options need to be available for those on chip functions that DFT seems prohibitive for. Most of these requirements fit within but don't necessarily drive open architectures. Open architectures may be the solution for very specialized function requirements.

The look of the future ATE industry is unclear. Will they take advantage of EDA alliances to move into the DFT realm? Offering DFT solutions, which are fabricated on chip and work in conjunction with ATE, to keep costs down is attractive. Does this require DFT “standards” or will these DFT functions have “ATE brands” on them, which limit their usage to particular ATE systems.

Will the ATE industry “level off” in performance at the interface speeds dictated by today's packaging and instead focus on cost reduction and competition with existing installed tester bases. At this point, the answers to these questions seem unclear and will be an interesting discussion topic.