

DESIGN VERIFICATION PROBLEMS: TEST TO THE RESCUE?

Prab Varma

Veritable Inc., Mountain View CA 94040, USA

The problems of generating manufacturing test vectors and design verification have some similarities that have led to test generation techniques being proposed for verification problems such as equivalence checking, property checking and design error test generation. There have been some successes in applying ATPG techniques to these problems. However, much progress still needs to be made.

Combinational ATPG has been used successfully for many years as one of the techniques employed by commercial equivalence checking tools to tackle the problem of verifying that two design representations are equivalent.

Recently, assertion based verification or property checking has become of great interest to the industry. Property checkers attempt either to prove that a specified property, which stipulates expected design behavior, holds or, if the property does not hold, to generate a counter-example that demonstrates a violation of the property. This is another area where there have been some promising successes in recent years, with sequential ATPG techniques finding their way into commercial property checking tools.

Traditional BDD based property checking approaches suffer from the state-explosion problem. ATPG/SAT techniques do not suffer from this problem to the same extent since they allow space to be traded for time. As a result they have been used to verify properties over a bounded number of cycles. In test generation for faults introduced during the manufacturing process, only a single test sequence that detects the fault is required. In design verification, to show that a bug exists, it is sufficient to search for a single valid test sequence that uncovers incorrect design behavior. However, all relevant portions of the state space, must be searched to prove that the design is correct. Thus, while ATPG techniques have been found useful in uncovering design bugs in bounded property checking, they are not, generally, used to try to prove properties over an unbounded number of cycles.

Despite some successes in formal verification, simulation is still the most widely used verification method and is

unlikely to be replaced by formal verification in the near term. There is still much research that needs to be performed in the area of simulation based verification. One area where there seemed to be initial promise, ATPG for design errors, has many problems that must still be overcome. Although commercial tools for design error test generation for RTL designs exist, acceptance of such tools has been limited. Some of the issues that have to be addressed are discussed below.

Manufacturing test is a structural test targeted at the gate level and as such does not have to generate vectors that are functionally valid. However, design verification, in general, must target RTL and must focus on the generation of sequences that are valid functionally. The generation of invalid sequences can be performed relatively easily using random techniques and is only necessary to prove that the design behaves as specified to incorrect inputs.

In manufacturing test, the manufactured IC is tested against the golden simulation model. In design verification the RTL that is to be verified is usually the golden model and behavioral models rarely exist. Where one does exist, it is unlikely to be cycle accurate. The lack of a golden model to check against is a major hurdle to the acceptance of design error ATPG. The relevance of current proposed design error models is also problematic and their effectiveness in detecting real design errors is generally questioned by designers.

In manufacturing test, a single test per fault is usually considered sufficient but in design validation each potential error should be detected many times under different conditions. One impact of the need for multiple detection is the increase in, already excessive, ATPG times. The significantly higher performance of biased/directed random techniques makes it likely that they will continue to be preferred for test generation.

Many challenges and opportunities exist for further research. A promising new direction for property checking is the use of ATPG in searching for sets of states in pre-image/image computation, while the most promising direction for design error ATPG is in targeting design properties under functional design constraints.

ITC INTERNATIONAL TEST CONFERENCE