

Open Microphone – My DFT is better than yours ...

In the world of Design-for-Test (DFT), experts often have strong, but contradicting, opinions on what the best methodologies are to best handle testing of today's ASICs and SoCs. In this open microphone panel, the audience is invited to discuss some of these controversies with experts from the semiconductor and EDA industries.

DFT to a large degree is based on models and theories. It is difficult to conduct research studies that truly determine the effectiveness of one methodology over another. As a result, there are many areas where experts have very strong preferences, and where, to the outside observer, there does not seem to be clear scientific reasoning for these preferences. Such areas include:

- Effectiveness of IDDQ. Will this methodology ever retire? If so, what should take its place?
- Structural test method for regular logic: ATPG vs. LBIST. Which methodology is preferred, especially with respect to:
 - o Overall test quality
 - o The best choice for at-speed test
 - o Test cost
- Best techniques for AC test
 - o Launch off shift vs. broadside launch
 - o Fault model (path delay, transition, others?)
 - o ATPG vs BIST
- DFT for SoC – fact or fiction. Will pattern reuse ever exist?
- Are structural patterns good enough, or is there and will there always be a need to supply functional patterns

This is a broad range of topics, but the intention of the debate is not to come up with an answer or ideal solution for each of these areas. For that, the issues are too many and too complex (and there are other sessions that are better suited for presentation of scientific studies.) Rather, the goal is to have the audience and the panelists engage in a lively and informal discussion regarding these topics so that the pro and con reasoning, and the consequences of the choices, can be well understood. Additionally, the debate will hopefully broaden the participant's insight into the variety of DFT methodologies and alternatives available.

Organizer: Geir Eide, Teseda

Moderator: Ken Posse, Teseda

Panelists: Experts from the ITC Audience