The Increasing Importance of On-line Testing to Ensure High-Reliability Products

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It is becoming more challenging to achieve very high reliability for products made with advanced technologies (90nm and smaller). [International Technology Semiconductor Roadmap, 2002] There are a variety of reasons for this trend--a brief summary is included below. This trend will force IC manufacturers to adopt new test and stress methods and to improve product reliability using system architecture enhancements—including the use of extensive on-line testing. In this summary paper, I will describe the key problems driving this change and describe some of the methods that can be used to improve final product reliability.

I believe that **many of the same methods used to improve testing at the chip and package can be used to improve reliability at the system level**. In fact, if such methods are not used there is likelihood that products may become less reliable over time—which is not acceptable to many applications.

The issues that make it more difficult to screen all defects during wafer or package-level testing include:

- ***There is an increase in subtle, hard-to-detect defects for advanced technologies.*** *Such defects include resistive vias, resistive shorts and implant deformations. These defect types may cause only minor performance abnormalities that are very difficult to exhaustively detect using state-of-the-art test methods. Such defects may cause only a few picoseconds of delay, for example.*
- ***Subtle defects (such as resistive vias) may degrade with use and are not stressed well by conventional methods (relying on voltage and temperature acceleration) such as burn-in****. These defects may only be accelerated by current density changes requiring many cycles of applying various circuit states to the device. Difficulty in stressing these defects will drive manufacturers to improve their test methods—enabling these defects to be detected rather than accelerated.*
- ***The effectiveness of stress methods for reliability-type defects is degrading.*** *For example, the difference in voltage between the application and high-voltage stress testing is decreasing for advanced technologies – causing an exponential decrease in stress effectiveness. Burn-in stressing is becoming problematic due to very high leakage currents at burn-in. IDDQ testing is becoming less effective due to increasing leakage currents.*
- ***The margin between the application condition and where the device actually operates is eroding.*** *For 0.18um products, there was often 1 Volt of margin between the design target VDD voltage and the minimum functional VDD at test (at slower conditions). For 90nm, this margin may shrink to less than 200mV. Many applications will have reduced margins for other parameters than VDD voltage (such as temperature & speed) which may lead to more intermittent failures.*
- ***Reliability-type failures may soon be caused by "expected" performance degradations such as Negative Bias Temperature Instability (NBTI).*** *Given these expected degradations, IC suppliers must decide how to account for devices slowing down. Regardless, on-line testing that can monitor performance will be a significant improvement in monitoring for these degradations.*

The problems mentioned above will **force many applications to adopt new solutions to improve product reliability over previous generations.** Although it isn't clear what all of these solutions will be, they will include:

- *More thorough testing at the chip/package level. (Leading to additional yield loss.)*
- *More focus on performance and margin-based testing.*
- *New testing & stressing methods aimed at problematic, subtle defect mechanisms.*
- *Additional guardbands to be verified at test to ensuring shrinking margins to not cause reliability failures.*
- *More use of error correcting methods (including logic error correcting)--including repair capability during the system application.*
- *Periodic testing of components to check for reliability defects or performance degradations. Such tests must check for environmental condition changes such as voltage margin and temperature drift.*

An interesting issue is "what methods will be used to periodically test IC components?" I believe that the applied methods will be similar to **the direction of IC testing – i.e., memory built-in self-test and logic built-in self-test using on-chip clock generation.**

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